INSTRUCTION MANUAL

MODEL 859-S-777

PROGRAMMABLE PULSE GENERATOR

WAVETEK

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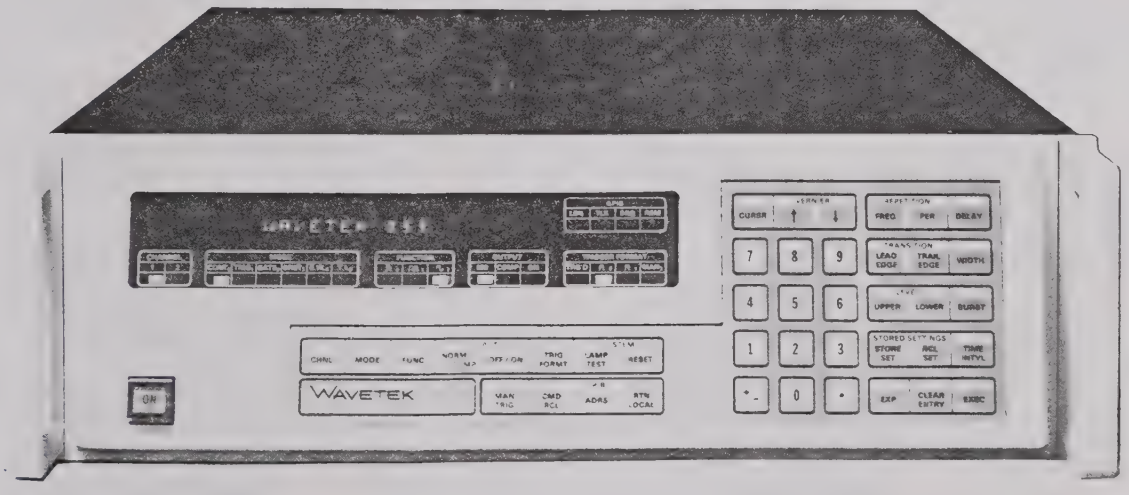


Model 859 Programmable Pulse Generator

SECTION 1
GENERAL DESCRIPTION

1.1 THE MODEL 859 AND OPTIONS

1.1.1 Standard Model

The Model 859, 50 MHz Programmable Pulse Generator, is a source of electrical pulses that can be programmed from the front panel keyboard or via a GPIB.

Pulse period, width, delay, levels and transition times are programmable. A vernier control allows real time incrementing and decrementing of these output pulse parameter values.

The generator can be programmed to operate in continuous mode or one of five triggered modes. Triggering may be by an analog signal, GPIB command or front panel key.

Up to 25 complete sets of programming may be stored and rapidly recalled.

1.1.2 Second Channel Option

A second channel of output is optional. All parameters are independent of the first channel, except frequency and mode.

1.2 SPECIFICATIONS

1.2.1 Versatility

1.2.1.1 Pulse Outputs

There are four pulse outputs.

1. Variable main channel pulse.
2. Second channel variable pulse (optional).
3. TTL compatible fixed sync pulse at lowest frequency in generation system.
4. Fixed symmetrical TTL compatible (approximately 50% duty cycle) clock output which follows repetition rate generator.

1.2.1.2 Operational Modes

Continuous: Output continuous at programmed frequency.

Triggered: Output quiescent until triggered for one single or double pulse.

Gated: As triggered mode, except repetition rate generator is enabled for duration of input trigger. Last pulse period started is completed. Maximum gate rate is 25 MHz.

Burst: As triggered mode, except repetition rate generator is enabled for programmed number of pulse periods from 1 to 10,000.

External Width: Trigger duration and rate set pulse width and repetition rate.

Time Interval: Trigger causes one pulse with programmed width: 20 ns to 9999s.

Resolution: To nearest 20 ns, <100 μs. To 4 digits, ≥ 100 μs.

Accuracy: 2% ± 2 ns.

Duty Cycle: 90% limited by 100 ns off time.

1.2.1.3 Pulse Functions

Single: One pulse each pulse period. Up to 50 MHz repetition rate.

Double: One pair of pulses each pulse period. Up to 25 MHz repetition rate. Both pulses have programmed width. Position of second pulse set by delay control.

Square: Pulse is fixed symmetrical (50% duty cycle) up to 50 MHz repetition rate with variable transition times to <5 ns.

50% $\pm 2\%$ ± 2 ns to 25 MHz.

50% $\pm 10\%$ ± 2 ns at >25 MHz.

Inhibit: Disconnected output and no error checking on channel.

1.2.2 Pulse Outputs

1.2.2.1 Main Output

Upper and lower pulse levels of both main output channels (second channel optional) are independently programmable. High impedance or 50Ω source impedance automatically selected. If upper level, lower level or peak-to-peak amplitude is > |10V|, the 50Ω internal source is changed to high impedance. The values in table 1-1 are for a precision 50Ω load impedance.
Pulses of either output channel may be normal or complement. In complement, upper and lower levels are interchanged. Transition times remain as programmed.

Table 1-1. Pulse Output Specifications

Characteristics	High Impedance Source	50Ω Source
Upper Level Range	−12.00 to +20.00V	−9.96 to +10.00V
Lower Level Range	−20.00 to +12.00V	−10.0 to +9.96V
Resolution (digits of programmed value)	<3 digits (20 mV)	3 digits (10 mV)
Amplitude	8.00 to 20.00V	40 mV to 10V
Accuracy	3% program value ±1% ampl ±100 mV	2% program value ±1% ampl ±50 mV
Repeatability	Highly dependent upon cable length and load impedance	±1% ampl ±50 mV
Preshoot		±3% ampl ±10 mV
Overshoot & Ringing		±3% ampl ±10 mV

1.2.2.2 Sync Output

A pulse of approximately −0.6 to 3V from 50Ω source at lowest frequency in generator system.

1.2.2.3 Clock Output

A pulse of approximately −0.6 to 3V from 50Ω source, approximately 50% duty cycle and with programmed repetition rate in continuous, gated and burst modes. Repetition rate in time interval mode determined by microprocessor.

1.2.3 Time Domain

1.2.3.1 Repetition Rate

Frequency Range: 0.5 Hz to 50 MHz.

Period Range: 20 ns to 2s.

Resolution: 3 digits of programmed value.

Accuracy: 2% ±1 ns.

Repeatability: 2% ±1 ns.

Jitter: 0.1% ±50 ps.

1.2.3.2 Width

Width control affects pulses of the main channels.

Range: 10 ns to 999 ms.

Resolution: 1 ns from 10 ns to 19.999 μs; 3 digits of programmed value from 20 μs to 999 ms.

Accuracy: ±1% ±2 ns.

Repeatability: ±1% ±1 ns.

Jitter: ±0.1% ±50 ps width <1 μs; ±0.05% width 1 to 10 μs; ±0.005% width >10 μs.

Duty Cycle: 90% limited by 10 ns minimum off time (with 4 ns transition time).

1.2.3.3 Delay

Delay control affects pulses of the main channels.

Range: 0 ns to 999 ms.

Resolution: 1 ns from 0 ns to 19.999 μs; 3 digits of programmed value from 20 μs to 999 ms.

Accuracy: ±1% ±2 ns.*

Repeatability: ±1% ±1 ns.

Jitter: ±0.1% ±50 ps delay <1 μs; ±0.05% delay 1 to 10 μs; ±0.005% delay >10 μs.

Duty Cycle: 90% limited by 10 ns minimum off time for delay <25 ns and by 20 ns minimum off time for delay ≥25 ns (with 4 ns transition times).

1.2.3.4 Transition Time

For pulses of either main channel, leading and trailing edge transition times adjustable from 5 ns to 25 ms (10% to 90% points of programmed amplitude).

Transition Times: Variable to approximately 50:1.

Leading and trailing edge times must be in the same range:

4 ns to 100 ns;
50 ns to 2.50 μs;
500 ns to 25.0 μs;

5 μs to 250 μs;
50 μs to 2.50 ms;
500 μs to 25.0 ms.

Resolution: 3 digits of programmed value when both transitions are in the first 10:1 portion of their transition time range, decreasing to 2 digits at 50:1.

Accuracy: ±5% ±2 ns.

Repeatability: ±1% ±1 ns.

Linearity: ±3% for transitions >50 ns.

1.2.3.5 System Delays

Fixed trigger input to sync output delays for each mode.

Triggered: 60 ±10 ns.

Gated: 100 ±10 ns.

Burst: 100 ±10 ns.

External Width: 40 ±10 ns.

Time Interval: 80 ±10 ns.

1.2.4 Input Characteristics

1.2.4.1 External Trigger

Arbitrary trigger signals accepted. Rising or falling edge triggering selectable.

Trigger Point: −5 to +5V adjustable at rear panel.

Impedance: ~1 kΩ paralleled by 22 pF.

Width: 10 ns minimum.

Amplitude: 700 mV minimum to ±10V maximum.

Repetition Rate: 50 MHz maximum.

1.2.4.2 Manual Trigger

Front panel key. In gated and external width modes, output active while key depressed.

1.2.4.3 GPIB Trigger

ASCII J. In gated and external width modes, H signals end of active interval.

1.2.4.4 GPIB

IEEE 488-1978 compatible for direct connection to GPIB. Optical isolation. Capabilities are as follows.

Listener: AH1 and L4.

Talker: SH1 and T6.

Service Request: SR1.

Remote Local: RL1.

Device Clear: DC1.

Device Trigger: DT1.

Parameter	Typical Programming Time
Command Handshake	2 μs
Data Handshake	220 μs
Frequency	15 ms
Period	20 ms
Upper Level	20 ms
Lower Level	20 ms
Delay	15 ms
Width	18 ms
Leading Edge	35 ms
Trailing Edge	35 ms
Time Interval	10 ms
Mode	10 ms
Function	5 ms
Channel	7 ms
Trigger Format	5 ms
Normal/Complement	5 ms
Output ON/OFF	5 ms
Burst Number	8 ms
Trigger	3 ms
Store Settings	20 ms
Recall Setting	8 ms*
Next Setting	5 ms*
Previous Setting	5 ms*
Execute	20 ms*
GET	2 ms
Reset	50 ms
GET Mode	5 ms
SRQ Code	5 ms
Talk Message	5 ms
Terminator	8 ms
Gate OFF	2 ms

*2.5 ms when via GET.

Measurements made with HP 9825A controller. Times will vary with different controllers. Data rate will follow slowest listener on bus.

1.2.5 General

1.2.5.1 Features

Trigger Indicator: Indicates when generator is properly triggered or a burst or time interval is in progress.

Error Detection: Microprocessor detected errors are displayed or flagged via SRQ.

Vernier: Key controlled step or continuous incrementing of any pulse parameter. Cursor selects digit to be updated. Automatic over and under flow.

Nonvolatile Stored Settings: Twenty five complete front panel setups can be stored and recalled from internal memory. Thirty day backup time. Forty-five hour maximum recharge time. Expandable up to 100 settings.

Reset: Generator is returned to standard setup for confidence check.

Command Recall: Key controlled display of last 36 characters sent via GPIB interface or keyboard.

Return To Local: Key controlled return from remote GPIB to local front panel operation (subject to local lockout).

Manual Trigger: Key controlled trigger for triggered, gated, burst, external width and time interval modes.

1.2.5.2 Environmental

Specifications apply for 25 ±5°c after 30 minutes warm-up. Instrument will operate from 0 to 50°C, 0 to 10,000 feet at 25°C and from 0 to 95% relative humidity at 25°C.

1.2.5.3 Dimensions

Fits standard 48.3 cm (19 in.) rack. Dimensions behind front panel are 43.2 cm (17 in.) wide; 13.3 cm (5¼ in.) high; 58.4 cm (23 in.) deep. Supplied with rack mount adapters.

1.2.5.4 Weight

26.3 kg (58 lb) net; 32 kg (70 lb) shipping.

1.2.5.5 Power

90 to 105V, 108 to 126V, 198 to 231V or 216 to 252V; 48 to 66 Hz. Single channel, 200 VA. Dual channel, 250 VA.

1.2.6 Option

001: Additional Channel — Second channel of delay, width, transition times and output levels. Channels share operating mode and internal clock period only. All other functions and parameters are independent.

NOTE

Specifications apply with transition time set to minimum; with a 50Ω source driving a 50Ω load.

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

CAUTION

Do not mount this instrument by front panel alone. Slides or tray support is necessary to prevent instrument damage.

The generator can be used as a bench instrument or rack mounted. In either use, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (paragraph 2.2.5) to verify operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a 3 amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.

2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

Card Position	Input Vac	Fuse
100	90 to 105	3 amp
120	108 to 126	3 amp
220	198 to 231	1.5 amp
240	216 to 252	1.5 amp

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

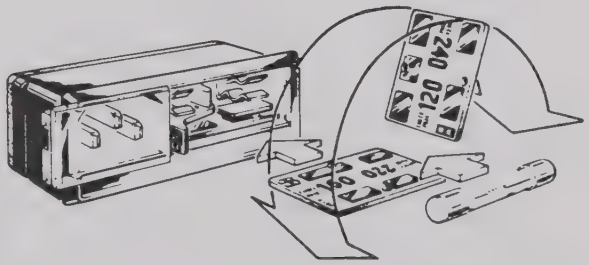


Figure 2-1. Voltage Selector and Fuse

2.2.2 Signal Connections

Use RG58U 50Ω coaxial cables equipped with BNC connectors to distribute signals when connecting this instrument to associated equipment.

TRIG IN BNC ±10V maximum, 1 kΩ impedance
SYNC OUT BNC 3V, 50Ω impedance
CLOCK OUT BNC 3V, 50Ω impedance
CH1 OUT BNC 20V into 50Ω load
CH2 OUT BNC 20V into 50Ω load
BNC ground may be floated a maximum of 42V peak.

2.2.3 GPIB Connections

The GPIB I/O rear panel connection is shown in figure 2-2; pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths). The GPIB interface is optically isolated from the instrument.

Table 2-1. GPIB Data In/Out

Pin	Signal	
1	DIO1	True When Low
2	DIO2	
3	DIO3	
4	DIO4	
5	EOI	
6	DAV	
7	NRFD	True When High
8	NDAC	
9	IFC	True When Low
10	SRQ	
11	ATN	
12	Safety Gnd	
13	DIO5	True When Low
14	DIO6	
15	DIO7	
16	DIO8	
17	REN	
18		Signal Gnd
19		
20		
21		
22		
23		
24		

2.2.4 GPIB Address

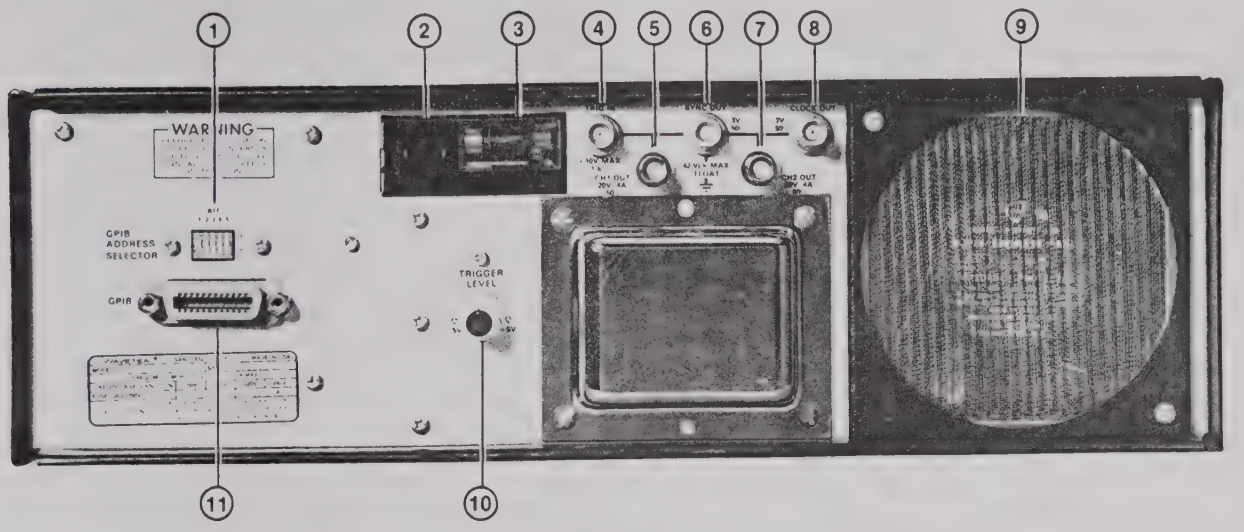
For instruments on the General Purpose Interface Bus (GPIB), ensure that the GPIB address is correct. The GPIB address can be changed by the switch on the rear of the instrument (see figure 2-2) by simply setting the multiple section switch according to table 2-2. The switch sections are labeled from 1 through 5 and their open positions are noted (OPEN = Binary 0 in table 2-2). To verify the address, press ADRS on the front panel. The device number (decimal) and ASCII listen and talk addresses will be displayed.

NOTE

Address 31 is not allowed.

Table 2-2. GPIB Address Codes

	Address								
	ASCII		Switch Position					Hexa-decimal	
Device	Listen	Talk	1	2	3	4	5	Listen	Talk
0	(space)	@	0	0	0	0	0	20	40
1	!	A	1	0	0	0	0	21	41
2	"	B	0	1	0	0	0	22	42
3	#	C	1	1	0	0	0	23	43
4	$	D	0	0	1	0	0	24	44
5	%	E	1	0	1	0	0	25	45
6	&	F	0	1	1	0	0	26	46
7	'	G	1	1	1	0	0	27	47
8	(	H	0	0	0	1	0	28	48
9	)	I	1	0	0	1	0	29	49
10	*	J	0	1	0	1	0	2A	4A
11	+	K	1	1	0	1	0	2B	4B
12	,	L	0	0	1	1	0	2C	4C
13	—	M	1	0	1	1	0	2D	4D
14	•	N	0	1	1	1	0	2E	4E
15	/	O	1	1	1	1	0	2F	4F
16	0	P	0	0	0	0	1	30	50
17	1	Q	1	0	0	0	1	31	51
18	2	R	0	1	0	0	1	32	52
19	3	S	1	1	0	0	1	33	53
20	4	T	0	0	1	0	1	34	54
21	5	U	1	0	1	0	1	35	55
22	6	V	0	1	1	0	1	36	56
23	7	W	1	1	1	0	1	37	57
24	8	X	0	0	0	1	1	38	58
25	9	Y	1	0	0	1	1	39	59
26	:	Z	0	1	0	1	1	3A	5A
27	;	[	1	1	0	1	1	3B	5B
28	<	\	0	0	1	1	1	3C	5C
29	=	]	1	0	1	1	1	3D	5D
30	>	↑	0	1	1	1	1	3E	5E



Location	Function	Paragraph
1	GPIB address selector DIP switch	2.2.4
2	Power cord receptacle	2.2.1
3	Fuse and fuse holder	2.2.1
4	Trigger signal input BNC	2.2.2, 3.7.2
5	Channel 1 output BNC	2.2.2, 3.9
6	Sync output BNC	2.2.2, 3.9.6
7	Channel 2 output BNC	2.2.2, 3.9
8	Clock output BNC	2.2.2, 3.9.7
9	Air filter screen	
10	Trigger acceptance level	3.7.2
11	GPIB connector	2.2.3

Figure 2-2. Rear Panel and Cross Reference

2.2.5 Initial Checkout and Operation

Make the equipment setup shown in figure 2-3 and perform the steps in table 2-3 to verify the 859 operation. Parameter letters on a lower corner of the keys are used to indicate the key to press. For example, program **P1I**.

P1I = OFF/ON (P) 1 EXEC (I)

Refer to appendix C for pulse parameter definitions. Refer to figure 3-1 if further keyboard or display explanations are required. Table 2-4, Acceptance Test Record, may be reproduced, completed and utilized as a record of acceptance.

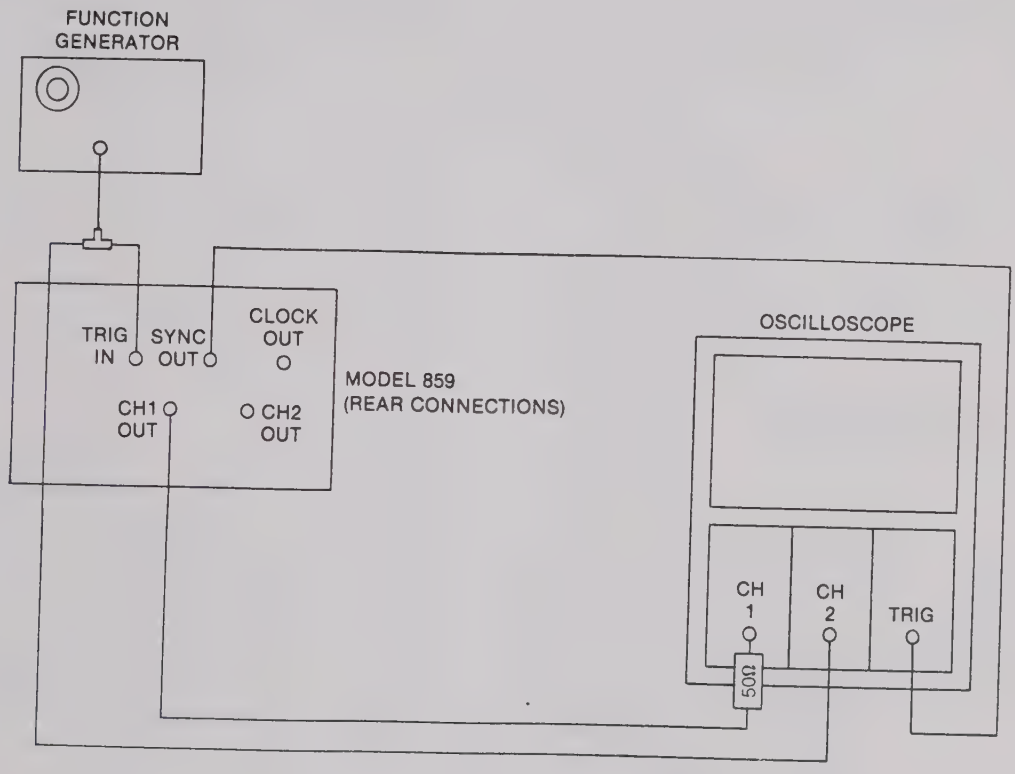


Figure 2-3. Equipment Setup

2.2.6 Performance Tests

Performance tests, table 2-5, verify that the parameters are within, or not within, specifications. Applicable portions of these tests should be used after equipment repair, and the entire test should be performed for assurance of signal quality. If an alignment problem is suspected, refer to section 6; if malfunction is suspected, refer to section 5. Refer to appendix C for pulse parameter illustrations.

NOTE

Allow instruments to warm up 30 minutes prior to tests.

Table 2-3. Operation Verification

Step	Test	Tester and Setup	Program	Desired Results
1	Self Test	None	Power: ON	859 displays *SELF-TEST* for less than 5s, then *WAVETEK 859*
2	Wake-UP State	Connect 859, oscilloscope and trigger source as in figure 2-3. Scope settings: CH1 0.5 V/Div CH2 0.5 V/Div Horizontal 0.2 ms/Div External trigger	Output: P1I	Scope: 1 kHz, 1 Vp-p square wave
3	Output Levels	Scope setting: CH1, 5 V/Div	Upper Level: A Press CURSOR and select Most Significant Digit (MSD). Press VERNIER ↑ until error occurs	Scope: Level increases positively
4			Upper Level: A 5I. Lower Level: D Press CURSOR and select MSD. Press VERNIER ↓ until error occurs	Scope: Level increases negatively
5			Reprogram levels: A10D0I	Scope: 10V upper level, 0V lower level square wave
6	Normal/Complement Output		Width: N3E-4 Function: C0I	Scope: 1 kHz pulse.
7			Complement Output: O1I	Scope: Complement of previous pulse
8			Output: O0I	Scope: Pulse width increases.
9	Width		Width: N1E-6IN Press CURSOR and select MSD. Press VERNIER ↑ until error occurs.	Scope: Pulse width increases.
10			Width: N20E-6I	Scope: 20 μs wide pulse
11	Delay		Delay: L1E-6II. Press CURSOR and select MSD. Press VERNIER ↑ until error occurs	Scope: Pulse delay increases
12	Leading Edge		Width: N3E-4 Delay: L1E-4. Transition Times: U1E-5V1E-5IU. Press CURSOR and select MSD. Press VERNIER ↑ until error occurs	Scope: Leading edge transition time increases.
13			Leading Edge: U10E-6I	Scope: 10 μs leading edge

Table 2-3. Operation Verification (Continued)

Step	Test	Tester and Setup	Program	Desired Results
14	Trailing Edge		Trailing Edge: V Press CURSOR and select MSD. Press VERNIER ↑ until error occurs	Scope: Trailing edge increases
15			Transition: U5E-9V5E-9I	Scope: 1 kHz pulse
16	Frequency	Scope setting: Horizontal 10 ms/Div; vary as needed. Normal triggering	Frequency: F1E1 Function: C2I Frequency: F Press CURSOR and select MSD. Press VERNIER ↑ until error occurs	Scope: Frequency increases.
17	Period	Scope setting: Horizontal 10 ms/Div; vary as needed.	Press CURSOR and select MSD. Press VERNIER ↑ until error occurs	Scope: Period increases
18	Double Pulse	Scope setting: Horizontal 0.2 ms/Div	Frequency: F1E3 Width: N5E-5 Delay: L60E-6 Function: C1I Press CURSOR and select MSD. Press VERNIER ↑ until error occurs	Scope: Delay of second pulse increases
19	Trigger Mode	859 TRIGGER LEVEL (Rear Panel) ~ 1V. Trigger source: 5 Vp-p, 1 kHz sine wave.	Mode: B1 Frequency: F1E4 Trigger Format: K0 Function: C0	Scope: A single pulse at the external trigger rate
20	Gated Mode	Scope settings: Auto trigger Horizontal 100 μs/Div	Trigger Format: K0. Function: C0. Width: N80E-6. Delay: L5E-8I Mode: B2I	Scope: A number of pulses occurring at the repetition rate during the active portion of the trigger signal
21	Burst Mode	Trigger source: 5 Vp-p, 10 Hz sine wave. Scope setting: Normal trigger Horizontal 2 ms/Div	Frequency: F1E3. Function: C2. Mode: B3. Burst: R10I	Scope: A burst of ten 1 kHz pulse occurring at a 1 Hz rate.
22	External Width Mode	Trigger source: 5 Vp-p, 1 kHz sine wave	Mode: B4 Trigger Format: K0I Vary 895 TRIGGER LEVEL control (Rear panel)	Scope: Observe output pulse width varies as trigger acceptance level varies.
23			Trigger Format: K1I Vary 859 TRIGGER LEVEL control	

Table 2-3. Operation Verification (Continued)

Step	Test	Tester and Setup	Program	Desired Results
24	Time Interval Mode	Scope setting: Internal auto trigger	Mode: B5 Trigger Format: K2 Time Interval: W10 Push MAN TRIG	Scope: a pulse output of 10s duration
25	Example Class 1 Error	None	Reset: Z Upper Level: A25I	859 display: *UPPR AMPL ERROR*
26			Upper Level: A	895 display: *UPPR AMPL 500 mV*
27	Example Class 2 Error		Reset: Z Mode: B1I	859 displays: *ERR CH1 TGSQ*
28	GPIB Interface	HP9825 Calculator. Connect to 859 GPIB connector. Set 859 rear panel address switch to 00001.	Press ADRS key	859 display: *GPIB ADDR 1 ! A*
29			Calculator Program 0: dim A$ [32] 1: dev "859", 701 2: wrt "859", "Z" 3: stp	859 displays: *859 RESET*
30			4: wrt "859", "F50E6" 5: stp	859 displays: *FREQ 50 MHz*
31			6: wrt "859", "%T3F" 7: red "859", A$ 8: dsp A$ 9: stp	9825 displays: *V FREQ 50E6*
32			10: clr "859" 11: stp	859 displays: *859 RESET*
33			12: wrt "859", "%Q1F0F" 13: rds ("859") → A 14: if bit (6, A) = 1; dsp "SRQ WORKING"; gto "STOP" 15: dsp "SRQ NOT WORKING" 16: "STOP": 17: stp	9825 displays: *SRQ WORKING*
34			18: wrt "859" "ALMOST DONE" 19: stp	Push CMD RCL on 859. 859 displays: *ALMOST DONE*
35			20: wrt "859", " 'TEST DONE' " 21: stp	859 displays: *TEST DONE*

Table 2-4. Acceptance Test Record
(for reproduction)

Location _____

QA Inspector _____

Date _____

Table 2-3. Step	Test	Channel (1) (2) Acceptable (✓)
1	Self Test	_____
2	Wake-Up State	_____
	Output Level	
3	Upper Level	_____
4	Lower Level	_____
6	Normal/Complement Output	_____
9	Pulse Width	_____
11	Pulse Delay	_____
	Transition Time	
12	Leading Edge	_____
14	Trailing Edge	_____
16	Frequency	_____
17	Period	_____
18	Double Pulse	_____
19	Trigger Mode	_____
20	Gated Mode	_____
21	Burst Mode	_____
22	External Width	_____
23	Time Interval	_____
	Error Checking	
24	Class 1 Errors	_____
25	Class 2 Errors	_____
26	GPIB Test	_____

Table 2-5. Performance Tests

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
1	Leading Edge	Scope (Figure 2-4)	Mode: B0 (cont) Function: C2 (square) Output: O0 (normal) Output: P1 (on) Freq: F12E6 Upper Level: A5 Lower Level: D-5 Leading Edge: U4E-9 Trailing Edge: V4E-9I	3.0 ns	6.0 ns
2	Trailing Edge		*NOTE* *For minimum transition times program '4E-9' (4 ns).*	3.0 ns	6.0 ns
3	Upper Level Overshoot and Ringing			+4.69V	5.31V
4	Lower Level Overshoot and Ringing			−5.31V	−4.69V
5	Leading and Trailing Edge Accuracy	Time Interval Probes and Counter (figure 2-5)	Frequency: F1E5 Leading Edge: U1E-7 Trailing Edge: V1E-7I	93 ns	107 ns
6			Frequency: F1E3 Leading Edge: U1E-6 Trailing Edge: V1E-6I	948 ns	1.052 μs
7			Leading Edge: U1E-5 Trailing Edge: VIE-5I	9.489 μs	10.502 μs
8	Frequency Accuracy		Leading Edge: U4E-9 Trailing Edge: V4E-9 Frequency: F50E6I	46.7 MHz	53.74 MHz
9			Frequency: F33E6I	31.3 MHz	34.8 MHz
10			Frequency: F25.1E6I	24 MHz	26.3 MHz
11			Frequency: F10E6I	9.7 MHz	10.3 MHz
12			Frequency: F1E6I	980 kHz	1.02 MHz
13			Frequency: F10E3I	9.8 kHz	10.2 kHz
14			Frequency: F1E2I	98 Hz	102 Hz
15	Delay Accuracy		Function: C0 (single pulse) Frequency: F1E7 Delay: L10E-9 Width: N10E-9I	7.9 ns	12.1 ns
16			Frequency: F5E6 Delay: L10E-8 Width: N10E-9I	97 ns	103 ns

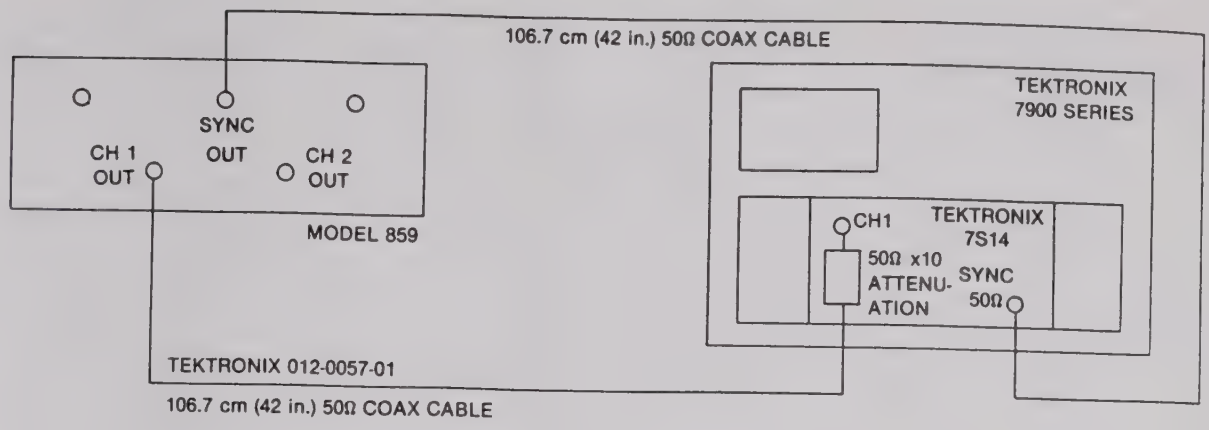


Figure 2-4. Model 859/Oscilloscope Test Setup

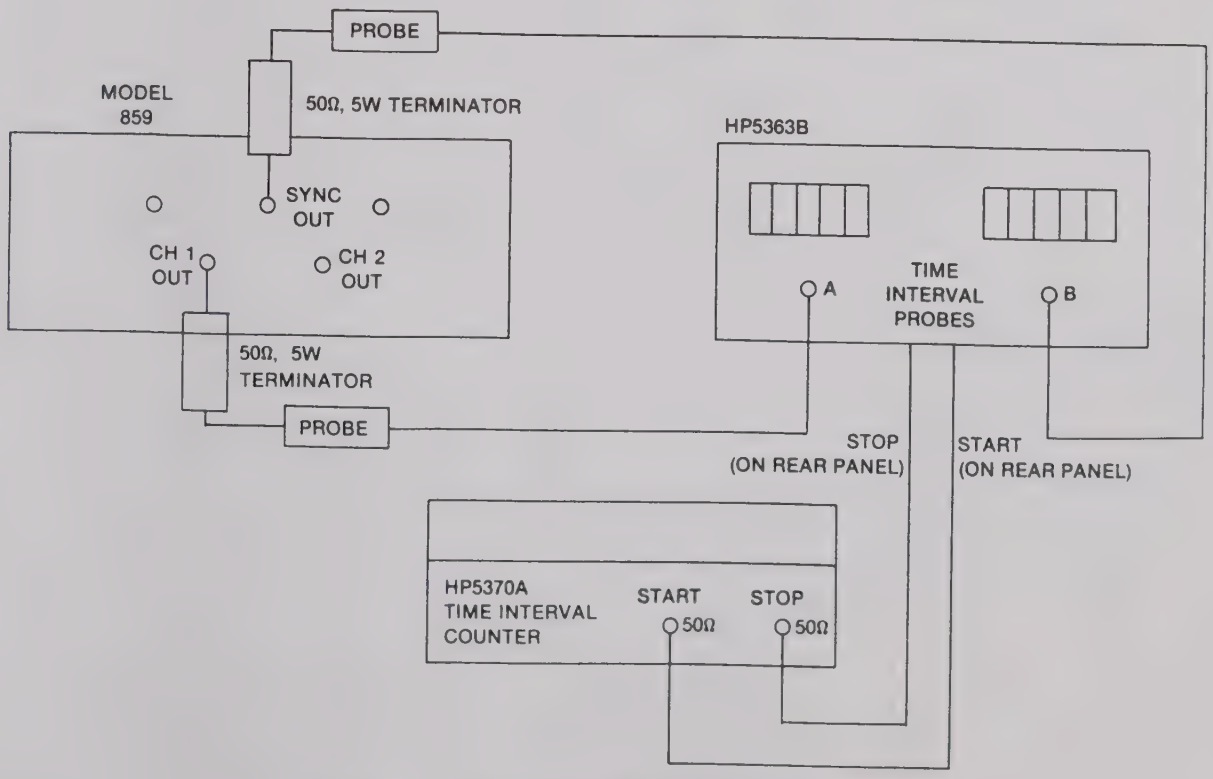


Figure 2-5. Model 859/Time Interval Probes and Counter Test Setup

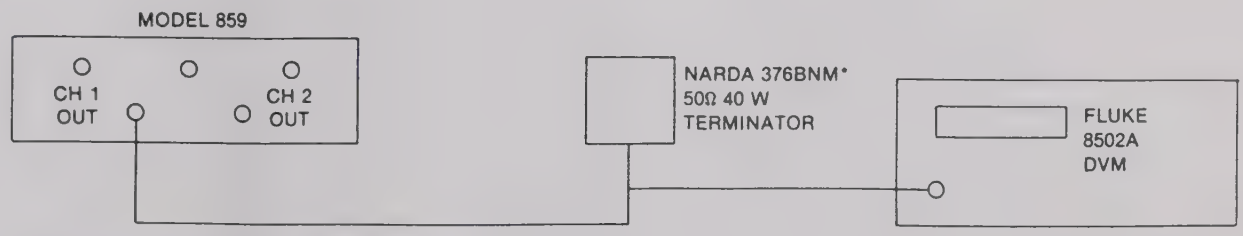
Table 2-5. Performance Tests (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
17			Frequency: F1E4 Delay: L10E-6 Width: N10E-6I	9.9 μs	10.1 μs
18			Frequency: F5E2 Delay: L1E-3 Width: N1E-3I	990 μs	1.01 ms
19			Frequency: F5E-1 Delay: L999E-3 Width: N1E-1I	990 ms	1.01s
20	Width Accuracy		Delay: L0 Frequency: F1E7 Width: N10E-9I	7.9 ns	12.1 ns
21			Frequency: F5E6 Width: N10E-8I	97 ns	103 ns
22			Frequency: F1E4 Width: N10E-6I	9.9 μs	10.1 μs
23			Frequency: F5E2 Width: N1E-3I	990 μs	1.01 ms
24			Frequency: F5E-1 Width: N999E-3I	990 ms	1.01s
25	Upper Level Accuracy	DVM (dc mode) (figure 2-6)	Mode: B4 (external width) Function: C2 (square) Output: O1 (complement) Trigger Format: K0 (lead edge) Lower Level: D0 Upper Level: A1E-1I	47 mV	153 mV
26			Upper Level: A2E-1I	144 mV	256 mV
27			Upper Level: A5E-1I	435 mV	565 mV
28			Upper Level: A1E0I	920 mV	1.08V
29			Upper Level: A2E0I	1.89V	2.11V
30			Upper Level: A5E0I	4.8V	5.2V
31			Upper Level: A1E1I	9.65V	10.35V
32			Upper Level: A2E1I	19.1V	20.9V
33	Lower Level Accuracy		Output: O0 (normal) Upper Level: A0 Lower Level: D-1E-1I	– 47 mV	– 153 mV
34			Lower Level: D-2E-1I	– 144 mV	– 256 mV
35			Lower Level: D-5E-1I	– 435 mV	– 565 mV

Table 2-5. Performance Tests (Continued)

Step	Measure	Tester & Setup	Program	Specified Range	
				Minimum	Maximum
36			Lower Level: D-1E0I	– 920 mV	– 1.08V
37			Lower Level: D-2E0I	– 1.89V	– 2.11V
38			Lower Level: D-5E0I	– 4.8V	– 5.2V
39			Lower Level: D-1E1I	– 9.65V	– 10.35V
40			Lower Level: D-2E1I	– 19.1V	– 20.9V

NOTE: If applicable, repeat steps 1 through 7 and 15 through 40 to evaluate the performance of channel 2.



*DVM READINGS MUST BE COMPENSATED FOR LOAD INACCURACIES (REF: PARAGRAPH 6.10)

Figure 2-6. Model 859/DVM Test Setup

Table 2-6. Performance Tests Record

Step of Table 2-5			Minimum	Maximum	Channel ___ (1 or 2) Actual Readings
	Leading Edge	Trailing Edge			
1	4 ns		1.8 ns	5.0 ns	_____
2		4 ns	1.8 ns	5.0 ns	_____

Overshoot and Ringing

	Upper Level	Lower Level			
3	5V		+4.69V	+5.31V	_____
4		−5V	−5.31V	−4.69V	_____

Leading Edge and Trailing Edge Accuracy

	Leading Edge	Trailing Edge			
5	100 ns		93 ns	107 ns	_____
		100 μs	93 ns	107 ns	_____
6	1 μs		9.489 ns	10.502 μs	_____
		1 μs	948 ns	1.952 μs	_____
7	10 μs		9.489 ns	10.50 μs	_____
		10 μs	9.489 ns	10.502 μs	_____

Frequency Accuracy

	Setting			
8	50 MHz	46.7 MHz	53.73 MHz	_____
9	33 MHz	31.3 MHz	34.8 MHz	_____
10	25.1 MHz	24 MHz	26.3 MHz	_____
11	10 MHz	9.7 MHz	10.3 MHz	_____
12	1.0 MHz	980 kHz	1.02 MHz	_____
13	10 kHz	9.8 kHz	10.2 kHz	_____
14	100 Hz	98 Hz	102 Hz	_____

Delay Accuracy

	Setting			
15	10 ns	7.9 ns	12.1 ns	_____
16	100 ns	97 ns	103 ns	_____
17	10 μs	9.9 μs	10.1 μs	_____
18	1 ms	990 μs	1.01 ms	_____
19	1s	990 ms	1.01s	_____

Width Accuracy

	Setting			
20	10 ns	7.9 ns	12.1 ns	_____
21	100 ns	97 ns	103 ns	_____
22	10 μs	9.9 μs	10.1 μs	_____
23	1ms	990 μs	1.01 ms	
24	1s	990 ms	1.01s	_____

Table 2-6. Performance Tests Record (Continued)

Step of Table 2-5		Minimum	Maximum	Channel ___(1 or 2) Actual Readings
Upper Level Accuracy				
	Setting			
25	0.1V	47 mV	153 mV	_____
26	0.2V	144 mV	256 mV	_____
27	0.5V	435 mV	565 mV	_____
28	1.0V	920 mV	1.08 mV	_____
29	2.0V	1.89V	2.11V	_____
30	5.0V	4.8V	5.2V	_____
31	10V	9.65V	10.35V	_____
32	20V	19.1V	20.9V	_____
Lower Level Accuracy				
	Setting			
33	0.1V	−47 mV	−153 mV	_____
34	0.2V	−144 mV	−256 mV	_____
35	0.5V	−435	−565 mV	_____
36	−1.0V	−920 mV	−1.08V	_____
37	−2.0V	−1.89V	−2.11V	_____
38	−5.0V	−4.8V	−5.2V	_____
39	−10V	−9.65V	−10.35V	_____
40	−20V	−19.1V	−20.9V	_____

SECTION 3
OPERATION

3.1 DATA ENTRY

Using the Model 859 is quite straight forward and is easily understood by trial and error method while the microprocessor "converses" with you during operation, informing you what was programmed, what is possible to program and when an error is made. The examples of data entry given in tables 2-3 and 3-1 will give you the feel of using the 859. Appendix B gives a summary of programming commands. Pulse waveform parameters are illustrated in Appendix C.

Use figure 3-1, Front Panel Cross Reference, to quickly find how a key functions or the significance of a particular display. Use table 3-2 and figure 3-2 as a guide to parameter programming for the mode in which you are operating.

Table 3-1. Front Panel Check of Initial Conditions

Instruction	Front Panel Key (Press Key)	Front Panel Display	Equivalent Program Entry
1. Power on.	OFF (becomes ON)	SELF TEST; then, within a few seconds, WAVETEK 859. Annunciator shows: CHANNEL 1 MODE CONT. FUNCTION ⌐⌙₂ OUTPUT 50Ω TRIGGER FORMAT MAN TRIGGER (2)	None
2. Check instrument address	ADRS	The state of the GPIB address switches will be displayed: GPIB ADDR 1, 2, 3 . . . or 30 (decimal address and ASCII listen and talk characters). Refer to paragraph 2.2.4 to change address.	None
3 Check initial conditions			
Channel	CHNL	CHANNEL 1 SELECTED	G
Mode	MODE	MODE CONT (0)	B
Function	FUNC	FUNC SQUARE (2)	C*
Output	OUTPUT NORM/COMP	NORMAL (0)	O*
Output	OUTPUT OFF/ON	OUTPUT OFF (0)	P*
Trigger Format	TRIG FORMT	MAN TRIGGER (2)	K
Frequency	REPETITION FREQ	FREQ 1 kHz	F

Table 3-1. Front Panel Check of Initial Conditions

Instruction	Front Panel Key (Press Key)	Front Panel Display	Equiv-alent Program Entry
Period	REPETITION PER	PERIOD 1 mSec	S
Delay	DELAY	DELAY 0 Sec	L*
Leading Edge	TRANSITION LEAD EDGE	LD EDGE 4 nSec	U*
Trailing Edge	TRANSITION TRAIL EDGE	TR EDGE 4 nSec	V*
Width	WIDTH	WIDTH 10 nSec	N*
Upper Level	LEVEL UPPER	UPPR AMPL 500 mV	A*
Lower Level	LEVEL LOWER	LOWR AMPL −500 mV	D*
Burst Length	BURST	BURST COUNT 2	R
Time Interval	TIME INTVL	TI INT 20 ns	W
Recall the program string	CMD RCL	GBCOPKFSLUVNADRW (this program string corresponds to all the last column entries)	None

*This parameter value is for channel one output. With two-channel generators, the second channel can have a different parameter value.

Table 3-2. Applicable Parameters In Each Mode

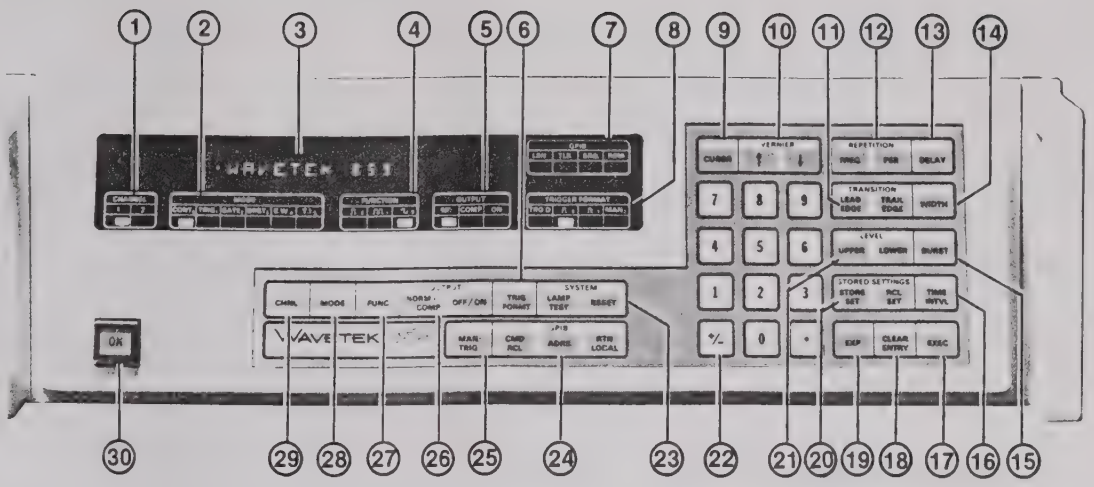
Parameter	Mode					
	Cont B0	Trig B1	Gate B2	Burst B3	EW B4	TI B5
Repetition (F or S)	✓	—	✓	✓	—	—
Transition (U and V)	✓	✓	✓	✓	✓	✓
Level (A and D)	✓	✓	✓	✓	✓	✓
Delay (L)	✓	✓	✓	✓	—	—
Width (N)	✓	✓	✓	✓	—	—
Burst (R)	—	—	—	✓	—	—
Time Interval (W)	—	—	—	—	—	✓
Channel (G)	✓	✓	✓	✓	✓	✓
Trigger Format (K)	—	✓	✓	✓	✓	✓
Func ⎍ (C0)	✓	✓	✓	✓	—	—
Func ⎍⎍ (C1)	✓	✓	✓	✓	—	—
Func ⎍ (C2)	✓	—	✓	✓	—	—
Output (O and P)	✓	✓	✓	✓	✓	✓

3.2 POWER

Power is turned on and off with a front panel push-button. When the power is turned on, the generator automatically performs a self test routine. "SELF TEST" is displayed at this time. When testing is completed, "WAVETEK 859" is displayed. At least two seconds must elapse between power OFF and power ON for proper reinitialization of logic. When the power comes on, the output is automatically disabled to allow loading of a program; line transients on the output are avoided. The generator must get an execute command to provide an output. (Refer to paragraph 3.5.)

3.3 BASIC COMMAND STRUCTURE

The Model 859 is programmed by sending ASCII coded characters (refer to Appendix A) to the microprocessor via one of the two possible input ports (keyboard or GPIB) shown in figure 3-3. If input characters are present on more than one input port, they are read first from the GPIB and then from the keyboard. Thus,



	Location	Function	Alpha Character	Paragraph
Annunciators	1	Channel		3.9.1
	2	Mode		3.7
	3	Readout		3.17
Annunciators	4	Function		3.6
	5	Output		3.9.2, 3.9.4
Key	6	Trigger Format	K	3.7.2
Annunciators	7	GPIB		3.11, 3.11.8
	8	Trigger Format		3.7.2
Keys	9	Cursor		3.12
	10	Vernier		3.12
	11	Transition Time	U/V	3.8.4
	12	Repetition	F/P	3.8.1
	13	Delay	L	3.8.3
	14	Width	N	3.8.2
	15	Burst	R	3.7.4
	16	Time Interval	W	3.7.6
	17	Execute	I	3.5
	18	Clear Entry		3.15
	19	Exponent		3.16
	20	Stored Settings		3.10
	21	Level	A/D	3.9.5
	22	Change Sign		3.3
	23	System		3.14
	24	GPIB		2.2.4, 3.11.1-3, 3.13
	25	Manual Trigger	H/J	3.7.2
	26	Output	O,P	3.9.2, 3.9.3
	27	Function	C	3.6
	28	Mode	B	3.7
	29	Channel	G	3.9.3
	30	Off/On		3.2

Figure 3-1. Front Panel and Cross Reference

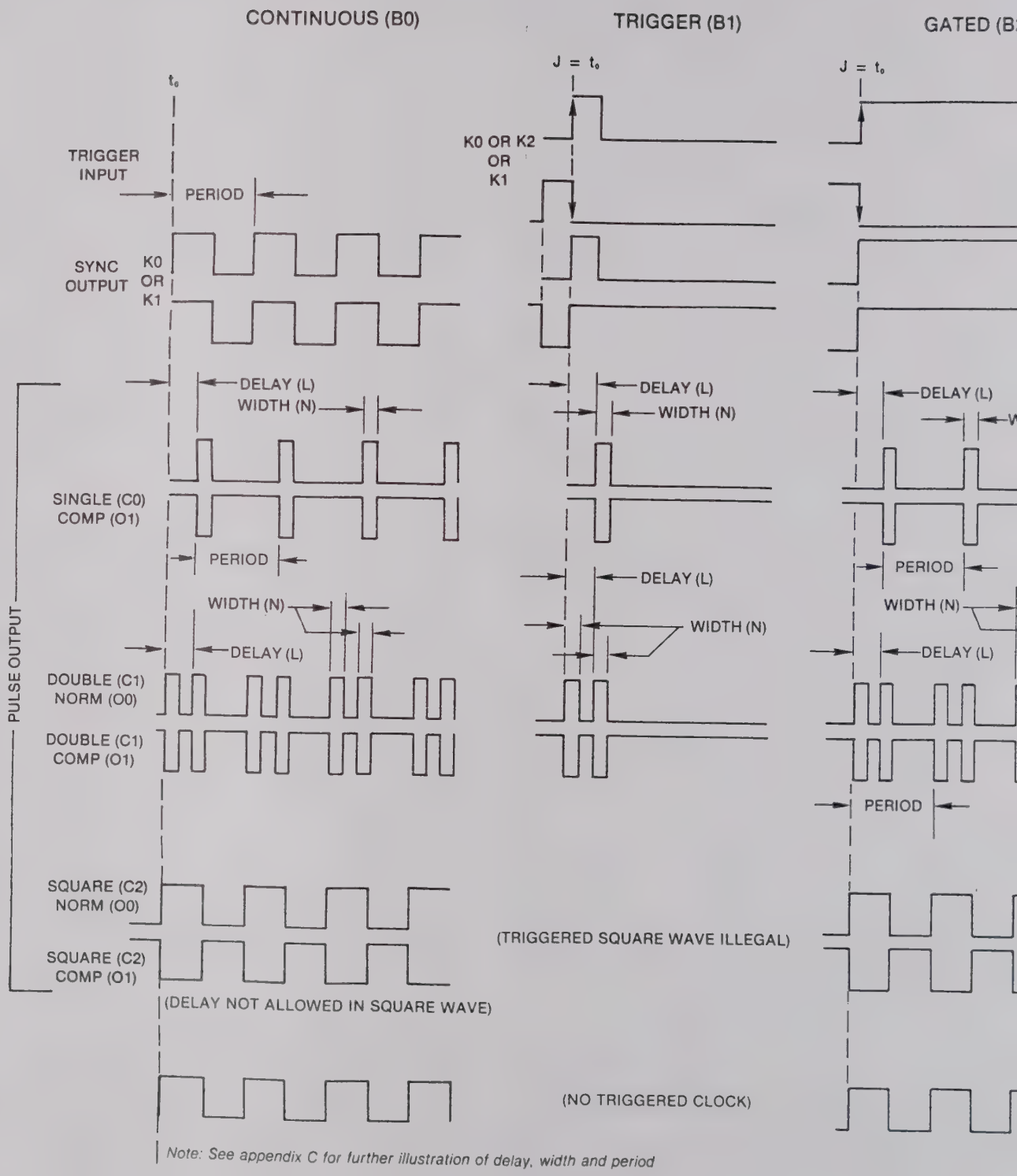
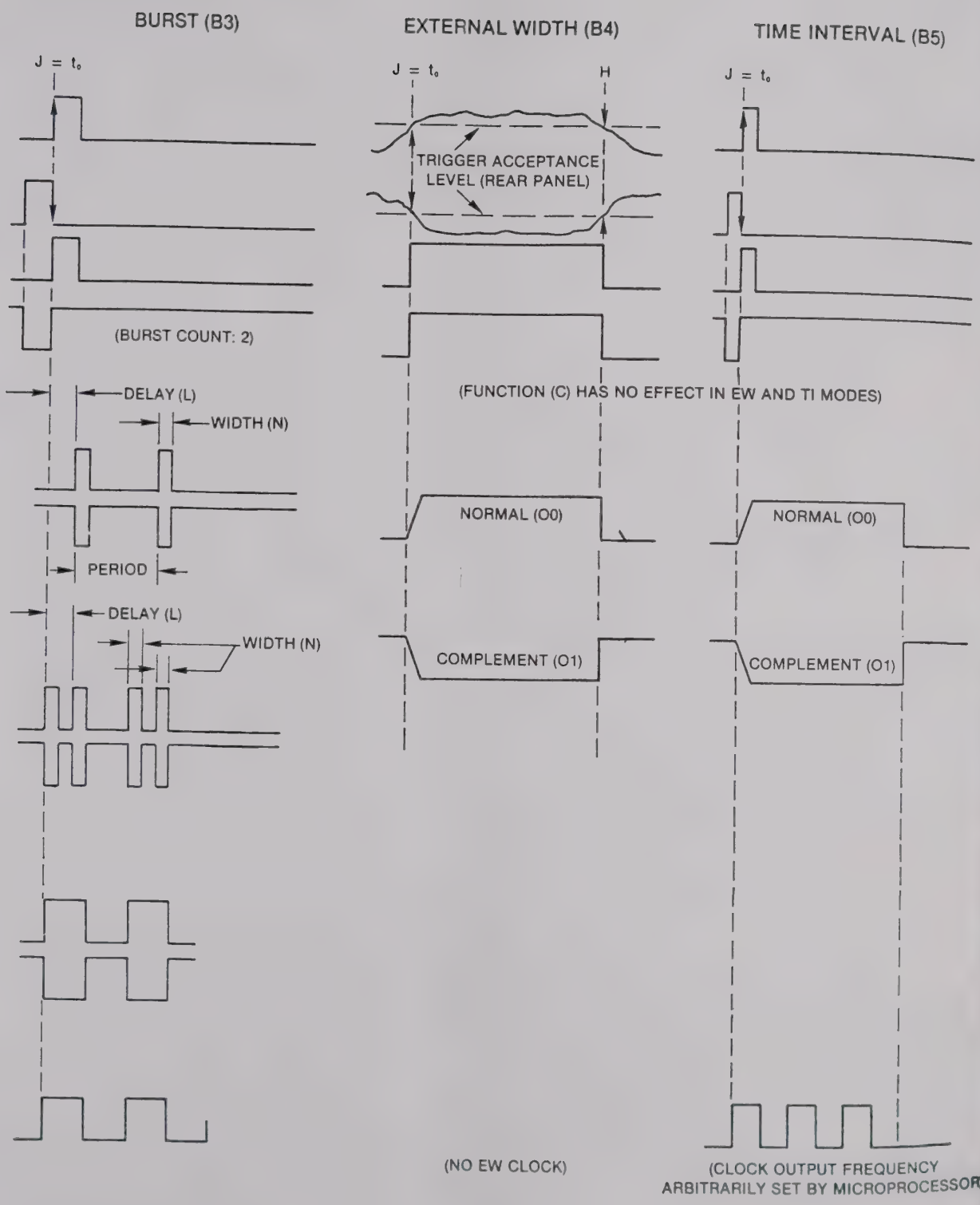


Figure 3-2. Output and Timing for Each Mode and Function


BURST (B3)
EXTERNAL WIDTH (B4)
TIME INTERVAL (B5)
J = t₀
H
TRIGGER ACCEPTANCE LEVEL (REAR PANEL)
(BURST COUNT: 2)
DELAY (L)
WIDTH (N)
PERIOD
DELAY (L)
WIDTH (N)
(FUNCTION (C) HAS NO EFFECT IN EW AND TI MODES)
NORMAL (O0)
COMPLEMENT (O1)
NORMAL (O0)
COMPLEMENT (O1)
(NO EW CLOCK)
(CLOCK OUTPUT FREQUENCY ARBITRARILY SET BY MICROPROCESSOR)

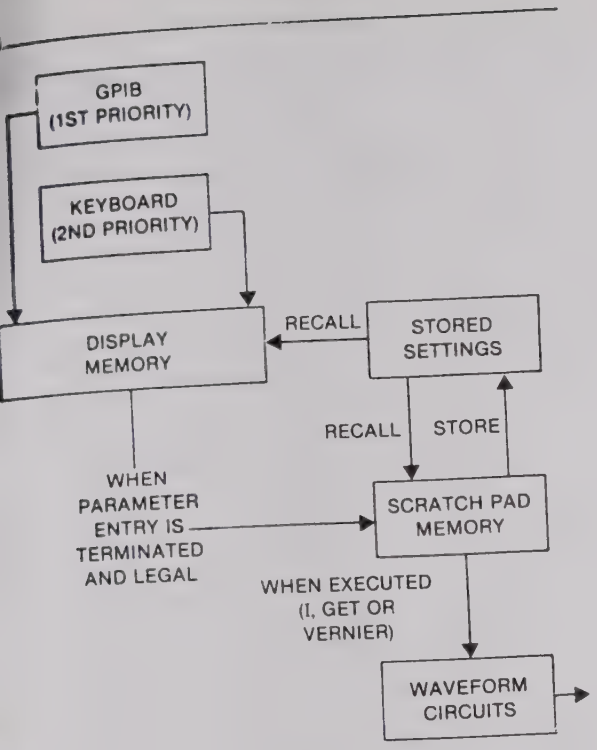


Figure 3-3. Memory Structure

if the GPIB port is continuously supplied with characters, then no characters will ever be read from the keyboard.

Characters used to program the 859 are divided into classes:

1. **Alphabetic Characters** — The characters A thru Z (except E) and the **%** character. The % character is used in front of an alphabetic character to select an alternate set of actions or commands. It must directly precede the alphabetic character with no intervening characters of any kind. For example, T selects the next stored setting, %T selects the talk message response, but %^T (where ^ is a space character) selects next stored setting, not talk message response, because a space character was placed between the % and the T. Alphabetic characters are generated from the keyboard by pressing the labelled action and parameter keys. The characters generated by such keys are printed in the lower corner of the key.

2. **Numeric Characters** — The characters 0 through 9, E, −, and decimal point (.).

3. **Special Character** — Quote (').

4. **Terminator Character** — Initially the ASCII line feed character (LF). This can be changed by programming.

5. **Nonprogramming Characters** — Any character not in one of the previously described classes. They have no effect on programming and may be interspersed freely among programming characters except after % (refer to item 1).

The alphabetic characters are used to select either actions or parameters. An action is a sequence of events which happens when the letter which selects it is programmed or the key that selects it is pressed. There is no need for a numerical suffix. A programming parameter has a letter (and a key) plus a numeric value which controls some aspect of the instrument's operation (refer to table 3-3).

Table 3-3. Alphabetic Characters Used in Model 859**

ASCII Character	Keyboard Key	Action/ Parameter	Comments
A*	LEVEL UPPER	P	Upper amplitude
B	MODE	P	Mode of operation
C*	FUNC	P	Waveform
D*	LEVEL LOWER	P	Lower amplitude
F	REPETITION FREQ	P	Repetition rate of waveform
G	CHNL	P	Channel 1 or (optional) 2
H	MAN TRIG (Release)	A	Gate reset
I	EXEC	A	Execute
J	MAN TRIG (Push)	A	Manual trigger
K	TRIG FORMT	P	Trigger format
L*	DELAY	P	Pulse delay
M	STORE SET	P	Store setting
N*	WIDTH	P	Pulse width
O*	OUTPUT NORM/COMP	P	Normal or complemented pulse
P*	OUTPUT OFF/ON	P	Output off or on

Table 3-3. Alphabetic Characters Used in Model 859 (Continued)

ASCII Character	Keyboard Key	Action/ Parameter	Comments
R	BURST	P	Number of pulses in burst
S	REPETITION PER	P	Pulse period (reciprocal of frequency)
T	——	A	Next stored setting
U*	TRANSITION LEAD EDGE	P	Pulse leading edge duration
V*	TRANSITION TRAIL EDGE	P	Pulse trailing edge duration
W	TIME INTVL	P	Time interval
X	——	A	Previous stored setting
Y	RCL SET	P	Recall stored setting
Z	SYSTEM RESET	A	Return to power-up setting
%G	——	P	GET mode of operation
%Q	——	P	Service request
%T	——	P	Talk message
%X	——	P	Terminator select

*This parameter's code or value can differ between channels of two channel instruments.

**Excluding the GPIB command groups, which are listed in appendix A.

To program an action, simply program the proper alphabetic character from either enabled port. The action will then take place, but only if the instrument is in the *enabled* state at the moment when that character is read by the microprocessor. (Refer to REN, paragraph 3.11.1, item 3)

To examine the current value of a parameter, simply program the proper alphabetic character from either input port. The current value will then be displayed on the front panel. This occurs whether or not the instrument is enabled. If the character programmed does not correspond to a legal parameter in the instrument, nothing happens.

The numeric characters (refer to table 3-4) are used to program new parameter values. To change a parameter value, first program the alphabetic character which selects the desired parameter (F = frequency, etc.). Next program the new value using numeric characters. Any sequence of characters which gives the new value is acceptable. For example, all of the sequences in table 3-5 will cause the value 100 to be programmed.

The numbers to the left of the E are the mantissa; the digits to the right (only two are allowed) are the exponent. The result value is the mantissa times 10 to the exponent power.

Table 3-4. Numeric Characters Used

ASCII Character	Keyboard Key	Function
0	0	Numeric digit
1	1	Numeric digit
2	2	Numeric digit
3	3	Numeric digit
4	4	Numeric digit
5	5	Numeric digit
6	6	Numeric digit
7	7	Numeric digit
8	8	Numeric digit
9	9	Numeric digit
.	.	Decimal point
–	+/–	Toggle sign
E	EXP	Indicates multiplication by 10 raised to a power

Only one decimal point and one E (keyboard EXP) are allowed per number; additional ones are ignored. The sign toggle character may appear any number of times. It causes the sign of the mantissa (if E has not been programmed) or the exponent (if E has been programmed) to be reversed (if negative, then positive,

Table 3-5. Examples of Value Programming

ASCII	Keyboard	Standard Notation
100	100	100
0100	0100	100 (leading zeros are ignored)
1E2	1 EXP 2	1×10^2
01E4	.01 EXP 4	$.01 \times 10^4$
01E304	01 EXP 304	$.01 \times 10^4$ (last two exponent digits only are used)
1000E-1	1000 EXP +/– 1	1000×10^{-1}
1E-2-	1 EXP +/– 2 +/–	1×10^2 (two minus signs cancel)
1E 2	1 EXP .2	1×10^2 (decimal points in exponent are ignored)

and vice versa) each time it appears. Any number of nonprogramming characters may be interspersed with the numeric characters, as they have no effect. If an undesired value is entered, the CLEAR ENTRY key can be used to erase it.

Several parameters require codes for specific selections; for example, function codes **0** through **3** select single pulse, double pulse, square wave and kill (no output and no error checking). Refer to table 3-6 for codes.

Table 3-6. Codes

Function (C) Codes	
0	Single Pulse
1	Double Pulse
2	Square Wave
3	Inhibit (no output, no error checking)

Mode (B) Codes	
0	Continuous
1	Triggered
2	Gated
3	Burst
4	External Width
5	Time Interval

Trigger Format (K) Codes	
0	BNC Rear Panel Connector, Rising Edge
1	BNC Rear Panel Connector, Falling Edge
2	Manual Trigger From Front Panel or GPIB

Output Normal/Complemented (O) Codes	
0	Normal
1	Complemented

Output Off/On (P) Codes	
0	Off
1	On

SRQ (%Q) Codes	
	NOTE *This parameter selects the conditions under which the GPIB SRQ signal will be sent by the 859.*
0	SRQ not sent
1	SRQ sent if a programming error occurred
2	SRQ sent upon completion of a waveform output in any mode except continuous.
3	SRQ sent if either of the events (1, 2) above occurs

Talk Message (%T) Codes	
	NOTE *This parameter selects which kind of message the 859 will send when it is addressed as a talker on the GPIB.*
0	Status of triggered indicator. H 1 is sent if the instrument is outputting a waveform in the triggered, burst or time interval mode. H 0 is sent if-not.
1	List of action and parameter selectors which caused programming errors. When read, this list is set to null.
2	Poll byte which would be sent in response to a GPIB serial poll.
3	Value of parameter selected by the most recently programmed selector.
4	State of waveform parameters common to both channels.
5	State of waveform parameters in channel 1.
6	State of waveform parameters in channel 2.

GET Mode (%G) Codes	
	NOTE *This parameter selects which kind of action the 859 will take when it receives a GET command.*
0	Execute and trigger upon receipt of GET command (no error checking).

Table 3-6. Codes (Continued)

GET Mode (%G) Codes (Continued)	
1	Fetch next stored setting, execute and trigger upon receipt of GET command (no error checking).
−1	Fetch previous stored setting, execute and trigger upon receipt of GET command (no error checking).

Since the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. This is done by programming either an alphabetic, special or terminator character. When this is done, the new value is rounded off (refer to table 3-7) and tested to see if it is a legal value for the setting being changed (refer to paragraph 3.4). If it is legal, the new value is entered into the instrument's scratch pad memory; however, it is not sent to the waveform circuits. That can be done only by programming the I action (EXEC key on the front panel). (Other methods of execution, GET and vernier, will be described later.)

Table 3-7. Round Offs

Parameter	Round Off
Upper Level (A) Lower Level (D)	To nearest 10 mV for $-10 \leq UL \leq 10$, $-10 \leq LL \leq 10$, and $UL - LL < 10$; otherwise to nearest 20 mV
Frequency (F)	To 3 digits
Period (S)	(Output to 3 digits)*
Delay (L) Width (N)	$<20\ \mu s$: to nearest ns, $\geq 20\ \mu s$: to 3 digits
Leading Edge (U) Trailing Edge (V)	<10 ns: to nearest 0.1ns, ≥ 10 ns: to 3 digits
Time Interval (W)	$<100\ \mu s$:to nearest 20 ns, $\geq 100\ \mu s$:to 4 digits
All Other Parameters	To nearest integer

*Refer to paragraph 3.8.1.

3.4 ERRORS

When an illegal value is programmed or interdependent parameter errors are detected, an error signal is indicated on the front panel or GPIB. Keyboard errors only are indicated on the front panel display and by a double "beep" of the key tone. For errors made via the GPIB (but not the keyboard), a service request (SRQ) is made, providing the service request function has been enabled (refer to paragraph 3.11.5). The controller can then serial poll its instruments to verify that the 859 sent the SRQ and can then inquire as to the nature of the 859 error. The method of reporting errors on the GPIB is given in paragraph 3.11.4.

3.4.1 Class 1 Errors

Class 1 errors are caused by programming values outside the legal limits of the parameter being programmed. For example, programming an upper level of 500 volts will cause a parameter error when the next alpha is programmed. At this time, the 859 disregards the new values and retains the previously programmed values in scratch pad memory (see figure 3-3).

3.4.2 Class 2 Errors

Class 2 errors are interparameter inconsistencies, such as pulse width greater than pulse period. Tests are made every time an execute (I) is commanded, a setup (M) is stored or a vernier key is pressed. Any resulting errors are displayed, and transfers of values are made to waveform circuits or storage regardless of the error indicated. Notice that upon receiving a Group Execute Trigger (refer to paragraph 3.11.7), the 859 programming will be executed without error checking.

In discussing the tests made, the following abbreviations are used:

UL — Upper Level	TE — Trailing Edge
LL — Lower Level	EW — External Width
LE — Leading Edge	TI — Time Interval

Tests always made are:

1. **UL/LL** — Amplitude error if $UL - LL > 20V$ or ($|UL| > 10$ or $|LL| > 10$) and $UL - LL < 8V$ or $UL - LL < 40$ mV.

2. **LE/TE** — Leading/trailing edge error if LE and TE settings are not in the same range. (Refer to paragraph 3.8.4.)

Additional tests depend on the mode and function parameters. The tests in one of the following groups (A through G) are performed depending on the current

value of the mode and function parameters. The particular test group to be used is given by this matrix:

	CONT	TRIG	GATED	BURST	EW	TI
⎍	A	F	A	A	—	D
⎍⎍	B	G	B	B	—	D
⎍	C	E	C	C	—	D

The test groups are listed as follows (an error condition is signalled if the associated condition is true).

A. W<< — Width too small if:

0.7 LE > Width − 0.625 TE.

W>> — Width too big if:

Width + 0.625 (LE − TE) ≥ 1.

D>P — Delay longer than period if (for delay <25 ns):

1.03 (Delay + 10 ns) > Period.

or if (for delay ≥25 ns):

1.03 (Delay + 20 ns) > Period.

W>P — Width longer than period if:

1.03 ([maximum of 1.3 TE or 8 ns] + Width + 0.625 [LE − TE]) > Period.

B. W<< — (Same as in group A.)

D<W — Delay shorter than width if:

1.02 ([maximum of: 1.3 TE or 8 ns] + Width + 0.625 [LE − TE]) > Delay.

D>P — (Same as in group A.)

D+W>P — Sum of delay and width longer than period if:

1.03 ([maximum of: 1.3 TE or 8 ns] + Width + Delay + 0.625 [LE − TE]) > Period.

C. LE>P — Leading edge longer than ½ period if:

1.935 LE > Period.

TE>P — Trailing edge longer than ½ period if:

1.935 TE > Period.

D. TI<LE — Time interval shorter than leading edge if:

1.1575 LE > TI.

E. TGSQ — Triggered square wave is always an error.

F. W<< — (Same as in group A.)

W>> — (Same as in group A.)

G. W<< — (Same as in group A.)

D<W — (Same as in group B.)

3.4.3 Class 3 Error

Class 3 error occurs if an empty stored setting is retrieved. The error will be displayed and the state of the 859 remains unchanged from the previously executed program.

3.5 EXECUTING THE PROGRAM

A program or setting can be executed; i.e., transferred to the waveform circuits by any of three methods: execute command, GET (Group Execute Trigger) command or vernier. (See figure 3-3.)

I or front panel EXEC key is an execute command that causes parameter value and interparameter tests to be made and transfers the programmed values to the waveform generation circuits.

GET is an exclusive GPIB command that combines several functions including execution and trigger, but without error checking. (Refer to paragraph 3.11.7)

Vernier, a front panel only function, includes digit increment, parameter value test, interparameter tests and an automatic execute. (Refer to paragraph 3.12.)

3.6 FUNCTION

A C followed by its function code selects the output pulse. Four function codes are used.

0 Selects a single pulse for each repetition rate period with a maximum rate of 50 MHz.

1 Selects double pulses for each repetition rate period up to 25 MHz.

2 Programs a square wave, with a maximum repetition rate of 50 MHz.

3 An inhibit condition which disconnects the output and suppress error checking on the channel selected.

Table 3-8. Output Signals Versus Mode

Mode	Channel Output	Clock Output	Sync Output
Continuous (B0)	⎍ ,⎍⎍, ⎍ 0.5 Hz to 50 MHz	⎍ 0.5 Hz to 50 MHz	⎍ 0.5 Hz to 50 MHz
Triggered (B1)	⎍ , ⎍⎍ at trigger frequency (⎍ not allowed)	Quiescent	Follows trigger input
Gate (B2)	⎍ ,⎍⎍ ,⎍ at internal period when gate is true	⎍ at internal period when gate is true	Follows trigger input
Burst (B3)	⎍ ,⎍⎍, ⎍ of 1 to 9999 at internal period	⎍ burst of n pulses, internal period	Follows trigger input
External Width (B4)	Follows trigger input	Quiescent	Follows trigger input
Time Interval (B5)	⎍ at trigger frequency	⎍ burst during time interval, internal period	Follows trigger input

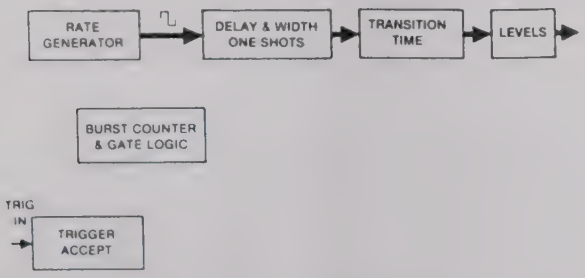
NOTE: ⎍ = pulse; ⎍⎍ = double pulse; ⎍ = square wave

3.7 MODE

Programming a B followed by its code (0 through 5) selects the operating mode. A front panel annunciator indicates the operating mode. Channel, clock and sync outputs for each mode are shown in table 3-8.

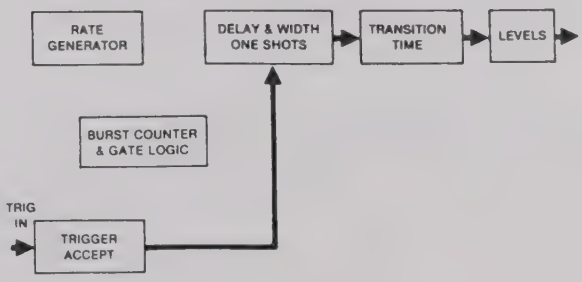
3.7.1 Continuous

B0 programs the continuous generation of output pulses. In continuous mode, the rate generator operates at the programmed repetition rate.



3.7.2 Triggered Mode, Format and Level

B1 selects the triggered mode. An external trigger will provide a single pulse output to 50 MHz, or double pulses to 25 MHz. The trigger signal level that is accepted by the 859 as a trigger is rear panel adjustable from −5 to +5 volts.



K followed by a code selects the trigger format to be used.

0 Causes the 859 to be triggered on the rising edge of the external trigger signal.

1 Causes the 859 to be triggered on the falling edge of the external trigger signal.

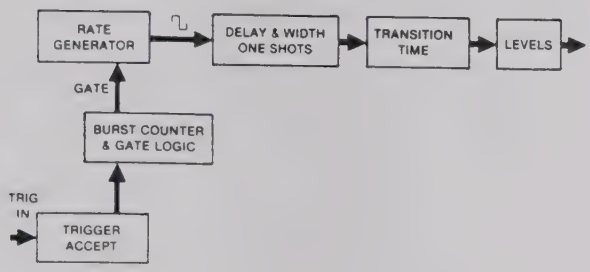
2 Selects manual trigger. Manual trigger operates from the front panel key or from the GPIB. Pressing MAN TRIG generates a single (or double) pulse each time the key is pushed. A similar trig-

gering action occurs via the GPIB; J is equivalent to pushing the key, and H is gate reset, which is the equivalent to releasing the trigger key.

An annunciator on the front panel (TRG'D) indicates when a trigger is present at the BNC input, GPIB or front panel manual trigger. When manual trigger is selected, inputs to the rear panel trigger input are ignored.

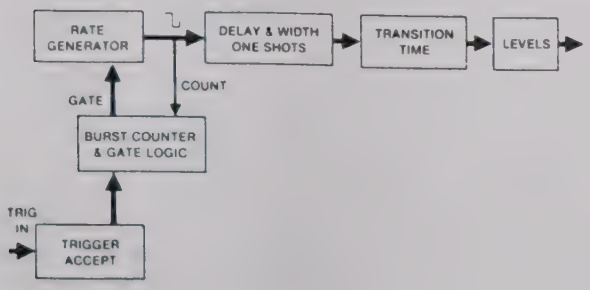
3.7.3 Gate

B2 selects the gate mode. In gate mode the trigger edge enables the rate generator for the duration of the trigger signal. The output is synchronous with the trigger signal and always concludes with a complete pulse cycle. Gate is a triggered mode requiring trigger format selection; refer to paragraph 3.7.2.



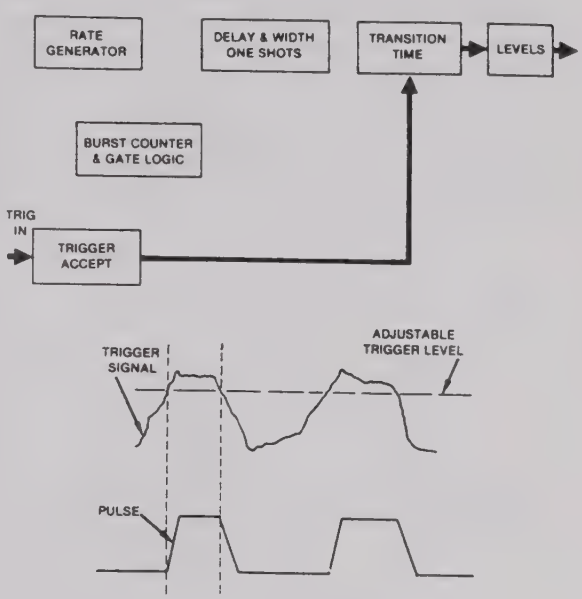
3.7.4 Burst Mode and Burst Length

B3 selects the burst length mode. Burst is a preprogrammed number of pulses at a preselected rate. R followed by its value, 1 to 9999, denotes the number of pulses in a burst. The duration of burst is dependent upon the programmed repetition rate. Burst is a triggered mode requiring trigger format selection; refer to paragraph 3.7.2.



3.7.5 External Width

B4 selects the external width mode. In external width mode, the output pulse period and width is fixed by the trigger signal, while transition time and output levels are adjustable by normal programming.

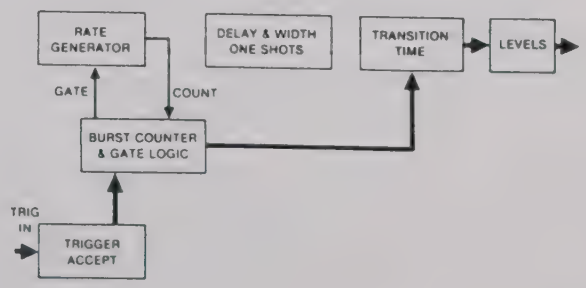


External width is a triggered mode requiring trigger format selection; refer to paragraph 3.7.2. The rear panel trigger level adjustment affects the width of the output pulse.

In manual trigger, the pulse width is between the manual trigger push and release, or J and H via the GPIB. The TRG'D annunciator indicates when the trigger circuit is active.

3.7.6 Time Interval

B5 selects the time interval mode. Time interval is a single output pulse of preprogrammed width duration. Levels and transition times are programmable.



Width of the time interval pulse is selected by programming W followed by its value. The time duration of the pulse is programmable from 20 ns to 9999 seconds (ref: table 3-7 for resolution). Time interval is a triggered mode requiring trigger format selection; refer to paragraph 3.7.2. The TRG'D annunciator indicates when the trigger circuit is active.

3.8 TIME DOMAIN

3.8.1 Repetition Rate

Repetition rate of the rate generator may be expressed by frequency or period. Frequency is programmable from 0.5 Hz to 50 MHz by programming F followed by its value in hertz. Frequency is programmable directly in hertz; for example F999, or scientific notation, for example F9.99E2. S followed by its value denotes the period in seconds. Periods are programmable from 20 ns to 2s, with three digit resolution. Internal to the 859, frequency is a dominant parameter; when a period is programmed, the 859 selects the nearest equivalent frequency. The actual pulse period is p = 1/f and will be displayed when the PER key is pressed. Rate generator programming does not affect the pulse output in trigger, external width and time interval modes.

3.8.2 Width

N followed by its value in seconds denotes the width of the programmed pulse. Pulse width is defined from the 50% point of the leading edge of the pulse to the 50% point of the trailing edge of the pulse. (As leading and trailing edge transition times are varied, the programmed pulse width is maintained.) Width is programmable from 10 ns to 1s. Resolution is three digits from 20 μs to 999 ms and 1 ns from 10 ns to 19.999 μs. Pulse width is limited to 90% of pulse period and a minimum of time determined by leading and trailing edge transition times; e.g., 10 ns for 4 ns transition times. Width programming does not affect output in external width and time interval modes and for the square waveform function.

3.8.3 Delay

L followed by its value in seconds denotes the pulse delay. Programmed pulse delays are from 0 ns to 999 ms with 1 ns resolution to 19.999 μs and 3 digits resolution to 999 ms. Delay is relative to the rising edge of the sync output. For the single pulse, delay is measured to the 0% point of the pulse. Delays for the double pulse are measured to the 0% point of the second pulse.

Delay limitations are expressed in terms of the delay one shot pulse (see figure 3-4). When using delay, the delay pulse is an internal pulse triggered at the start of the pulse period or triggered by the acceptance of an external trigger. The completion of this delay pulse starts the output pulse, or, in the case of the double pulse, starts the second pulse. The delay pulse duty cycle cannot exceed 90% of the pulse period. Additionally, for delays less than 25 ns, the off time of the delay pulse cannot be less than 10 ns and for delays greater or equal to 25 ns, the off time cannot be less than 20 ns.

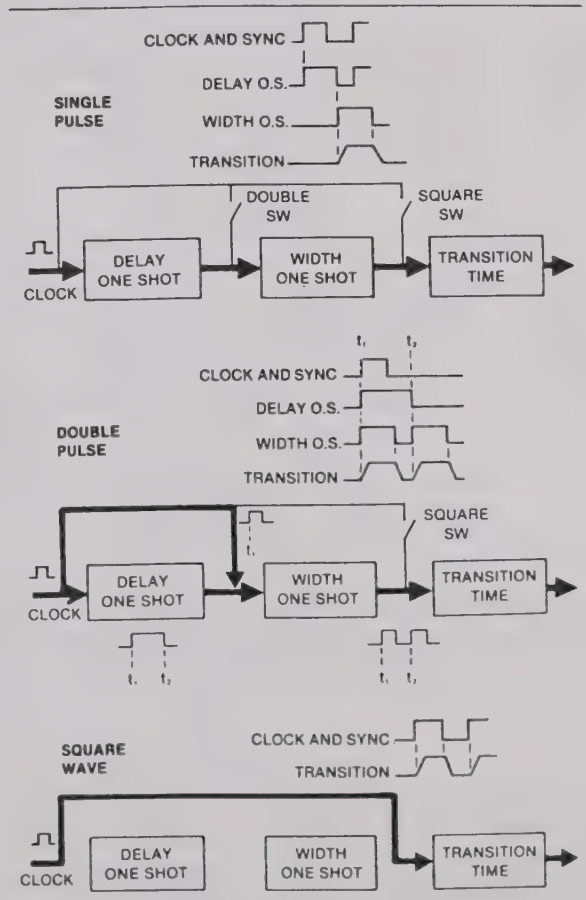


Figure 3-4. Function Determined Circuit Connections

3.8.4 Transition Times

U followed by its value in seconds programs the leading edge transition time. The trailing edge is pro-

grammed by V and its value in seconds. Transition times are measured from 10% to 90% points on the pulse edge and are programmable from 5 ns to 25 ms in six overlapping ranges:

4 ns to 100 ns
50 ns to 2.5 μs
500 ns to 25 μs
5 to 250 μs
50 μs to 2.5 ms
500 μs to 25 ms

Resolution is three digits when both transitions programmed are in the first 10:1 portion of their transition range and two digits resolution otherwise.

The microprocessor maintains the programmed pulse width (leading edge 50% point to trailing edge 50% point) in single pulse and double pulse functions.

3.9 PULSE OUTPUTS

3.9.1 Channel

A second main output, channel 2 is optional. For two channel 859's, pulse parameter programming subsequent to channel selection pertains to that channel. In addition, mode (B) and repetition (F, S) pertain to both channels.

At power up and reset times, channel 1 is automatically selected. A G followed by code 1 selects channel 1 and G followed by code 2 selects channel 2. Should a more than one digit code be entered, round off to one digit will occur.

3.9.2 Output Off/On

A P followed by a code switches the output on or off.

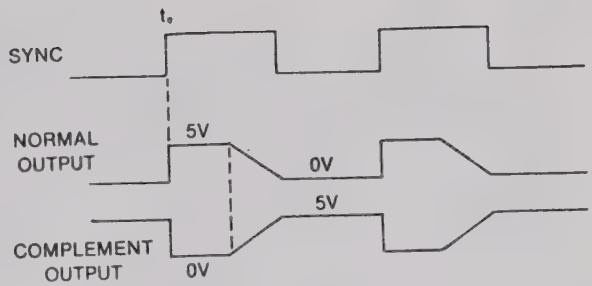
0 Internally disconnects the channel output from the rear panel BNC, making the signal unavailable.

1 Internally connects the signal to the rear output BNC, making the signal available.

3.9.3 Normal/Complement

An O followed by a code controls the phase of the output pulses relative to the sync output leading edge.

0 Selects the normal phase pulse output. At the t_0 time the output pulse will be positive going, for example.



1 Selects the complement phase of the output pulses. At the t_0 time the output pulse will be negative going, as shown above.

Pulse delay and pulse leading edge are related to the 0% point of the pulse as measured from the off level regardless of the normal/complement orientation of the pulse. Should a more than one digit code be entered, round off to one digit will occur.

3.9.4 Loads

All outputs in the 859 are specified into a 50Ω load. The 859 has two internal source impedances, 50Ω and a much higher impedance, which are automatically switched according to the programmed pulse levels. The 50Ω backmatch is maintained under the following criteria (annunciator shows 50Ω):

Upper Level Range:	−9.96 to +10.0V
Low Level Range:	−10.0 to +9.96V
Pulse Amplitude:	40 mV to 10V

When the level ranges or pulse amplitude range is exceeded, the 50Ω backmatch is dropped and the source impedance reverts to a high value.

3.9.5 Levels

An A followed by its value sets the upper level. The upper level has a voltage range of −12.00 to +20.0V. A D followed by its value sets the lower level. The lower level has a voltage range of −20.0 to +12.00V. Both the upper and lower level parameters have a resolution of three digits for levels of −10V to +10V, decreasing to 20 mV for levels outside this range. At the next programmed alpha character after a level value is programmed, the 50Ω backmatch is switched as described in paragraph 3.9.4.

3.9.6 Sync Output

Sync output is provided at a BNC on the rear panel. The sync signal is 0V to approximately 3V (TTL) from a 50Ω source. Sync output is a square wave in continuous mode. In other modes, sync width is determined by the time between the initial transition of the trigger signal through the preset trigger level to the trailing transition. For reference, refer to table 3-8, Output Signals Versus Modes, and table 3-9, System Delay Times. For best performance the sync output should be terminated into 50Ω.

Table 3-9. System Delay Times

Mode	Trigger Input To:*		
	Sync	Clock	Main Output**
Continuous (B0)	——	——	——
Triggered (B1)	60 ns	——	60 ns
Gate (B2)	100 ns	100 ns	100 ns
Burst (B3)	100 ns	100 ns	100 ns
External Width (B4)	40 ns	——	40 ns
Time Interval (B5)	80 ns	80 ns	80 ns

*All times ±10 ns
**Add programmed delay time to these fixed delays for actual time after trigger.

3.9.7 Clock Output

Clock output is provided at a BNC on the rear panel. The clock signal is 0V to approximately 3V (TTL) from a 50Ω source. Clock output is a square wave at the programmed repetition rate for continuous, gated and burst modes. In time interval modes, the clock rate is determined by the microprocessor. For reference, refer to table 3-8, Output Signals Versus Modes, and table 3-9, System Delay Times. For best performance the clock output should be terminated into 50Ω.

3.10 STORED SETTINGS

Up to 25 different sets of front panel settings can be stored in and recalled from Random Access Memory (RAM). Internal batteries allow power off storage for 30 days. Each stored set contains information specifying complete front panel parameters for two channels.

3.10.1 Storing Program Sets

Program sets may be stored by keyboard or GPIB command. To store a program set, enter parameter values and codes so that if the program were executed, output would be exactly as desired. (It is not necessary to actually execute the program.) Now enter **M** followed by the storage location (1 through 25). The next alpha programmed will act as a terminator. If a program was previously stored in that location, it will be erased and replaced by the new set. When a program is stored, the settings are tested for errors in the same manner as with an execute command (refer to paragraph 3.4). The program is always stored, whether or not errors were detected. Notice that programs can be stored without interrupting the output of the 859.

3.10.2 Recalling Programs

The information stored in a program may be recovered either from the front panel or by a command over the GPIB. To recall, program a **Y** followed by the number of the desired program. When the next alpha key is pressed, the settings stored in the selected program are transferred to the display memory and the scratch pad memory. Then data is available to be sent to the waveform circuitry of the instrument, or, if desired, it may be examined and possibly altered by use of the front panel keys.

The identifying numbers of programs in RAM range from 1 through 25. If the number of a program which does not exist or an illegal identifying number is programmed, an error will result.

Pressing the VERNIER ↑ key or programming **T** causes the program next in sequence after the last program accessed to be recalled. This provides an automatic way to recall a sequence of programs. However, the programs need not be numbered consecutively. If there is no program following the last program accessed, an error occurs.

Pressing the VERNIER ↓ key or programming **X** causes the previous program in sequence before the last program accessed to be recalled. This action works like the VERNIER ↑ (**T**) action previously described, except that programs are recalled in descending numeric order.

3.10.3 High Speed Recall of Programs

The Group Execute Trigger (GET) allows a rapid GPIB recall of stored programs in three modes. (Refer to

paragraph 3.11.7.) In the GET mode of operation, the program is recalled and executed, and the waveform circuits are triggered, all within 2.5 ms of receiving the GET command.

3.10.4 Deleting Programs

To delete a program, program the letter **M** followed by a *minus* sign and the number of the program to be removed. When the number is terminated, the program is removed from storage; there is no other effect.

3.11 GPIB

Almost all of the information in Section 3 is applicable to the General Purpose Interface Bus (GPIB) programming of the 859, but the information in this paragraph is *exclusive* to the GPIB.

The GPIB interface is an implementation of IEEE Standard 488-1978. It supports the following interface functions: Source Handshake (SH1), Acceptor Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL1), Device Clear (DC1) and Device Trigger (DT1). Devices connected to the GPIB can have one or more of the three capabilities: talk, listen and control. The talk capability allows a device to send data (such as voltmeter or counter readings) out over the bus. The listen capability allows a device to receive data (such as device programming information or a printer receiving data to be printed) from the bus. The control capability allows a device to control the flow of data over the bus. Although there may be more than one device connected to the GPIB with control capability, only one device at a time may exercise that capability on the bus. One device's control capability must be active at all times; this device is called the controller.

3.11.1 Bus Lines Defined

The GPIB consists of 16 signal lines:

DIO1 - DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

Their functions are:

1. **DIO1 - DIO8** — These eight lines (Data In/Out) are used to send commands and data encoded as 8 bit binary numbers (bytes).

2. **ATN** — This line (Attention) is operated only by the controller. It specifies whether the information on lines DIO1 - DIO8 is data (false) or a command (true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages; additionally, every device connected to the bus is required to receive and process every command sent by the controller.

3. **REN** — This line (Remote Enable) controls whether devices on the GPIB are in local or remote mode. In local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed: GPIB originated commands are obeyed, while front panel commands are ignored. A device enters the remote state whenever it receives its listen address (refer to paragraph 3.11.2.1) at the same time as REN is in the remote state. The device then stays in the remote mode until either the REN line is put in the local state or the device receives a Go To Local (GTL) command or the LOCAL front panel key is pressed while the interface is not in the local lockout state (refer to paragraph 3.11.2.4, item 4).

4. **DAV, NRFD, NDAC** — These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1 -DIO8. For each command or data byte transferred, a complete handshake cycle must occur. This handshake is designed to hold up the bus until the slowest device has accepted the information.

5. **EOI** — When ATN is false, this line (End Or Identify) indicates that the data on lines DIO1 - DIO8 is (true) or is not (false) the last byte of a data message. When the 859 receives a data byte with EOI true, it automatically supplies a terminator character (refer to paragraph 3.11.6) following the data byte. When the 859 transmits the last byte of a message (which is always a terminator character), it also sets EOI true.

6. **SRQ** — This line (Service Request) is used by the devices on the bus to signal the controller that they need attention. (Refer to paragraph 3.11.5

for 859 Service Request Enable.) Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signalling. The Serial Poll capability is usually employed to accomplish this.

7. IFC — This line (Interface Clear) is used by the controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.11.2 Commands

Commands are sent over lines DIO1 - DIO8 with ATN true. They are divided into five classes.

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands

   DCL — Device Clear
   SPE — Serial Poll Enable
   SPD — Serial Poll Disable
   LLO — Local Lockout

5. Addressed Commands

   GTL — Go To Local
   SDC — Selective Device Clear
   GET — Group Execute Trigger

These commands and command groups are shown with their binary codes in Appendix A and further explanation follows.

3.11.2.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1 - DIO8. There are 31 different available addresses (hexadecimal codes **20** through **3E**, ASCII codes **SP** through **>**). A 32nd address, called unlisten (hexadecimal **3F**, ASCII **?**), is used to command all devices not to read data bytes. The 859 listen address is selected by the rear panel switches, which specify the lower 5 bits of the address. (Refer to table 2-2.) Pressing the front panel ADRS key displays the GPIB address as a decimal device number followed by the ASCII character listen and talk addresses.

3.11.2.2 Talk Addresses

Talk addresses are used to command a device to transmit data over lines DIO1 - DIO8 whenever ATN is false. There are 31 different available addresses (hexadecimal codes **40** through **5E**, ASCII codes **@** through **^**). A 32nd address, called untalk (hexadecimal **5F**, ASCII **—**) is used to command all devices to cease talking. The lower 5 bits of the 859 talk address are selected by the same rear panel switches used to select the listen address. Thus, if the 859 listen address is hexadecimal **21** (ASCII **!**), the talk address is hexadecimal **41** (ASCII **A**). Pressing the front ADRS key displays the GPIB address as a decimal device number followed by the ASCII character listen and talk addresses.

3.11.2.3 Secondary Addresses

Secondary addresses are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the 859.

3.11.2.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the 859 are:

1. **Device Clear (DCL) —** Resets the 859 to the initial power on settings. Refer to table 3-1 for power on conditions. DCL affects all devices on the bus. This information is also set into the waveform generating circuitry.

2. **Serial Poll Enable (SPE) —** Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to an ASCII blank, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the 859 talk message number 2. When this message is read, the status byte is reset and SRQ released as for the serial poll.

3. **Serial Poll Disable (SPD) —** Discontinues serial poll. Returns instruments to normal talk modes.

4. **Local Lockout (LLO) —** Causes the GPIB interface to enter a state where the front panel LOCAL key is inoperative. Once in this state, the

only way to take the interface out of it is to put the REN line in the local state (refer to paragraph 3.11.1, item 3). Local lockout must be sent to the 859 to totally disable front panel modification of the state of the instrument.

3.11.2.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the 859 are:

1. **Go To Local (GTL) —** Commands the 859 to go to the local mode (refer to paragraph 3.11.1 for explanation of the REN line).

2. **Selective Device Clear (SDC) —** Resets the 859 to initial power on conditions. Refer to table 3-1 for power on conditions. SDC affects only the selected unit.

3. **Group Execute Trigger (GET) —** Causes the actions as specified by the GET mode (%G) code (refer to paragraph 3.11.7). If the 859 microprocessor is idle (i.e., not processing a previously sent programming string), a GET command will be completed within 2.5 ms of receipt. Otherwise, it will not be done until current programming is processed.

3.11.3 Data Transfer

In addition to accepting programming characters, the 859 will transmit status information over the bus. To program the instrument, first send the listen address (with ATN on), followed by the programming data (in ASCII, with ATN off). The instrument microprocessor accepts the data as fast as possible, until either 64 characters are received or there is a pause during the transfer of data. At that time, the entire string of received characters is scanned by the microprocessor, which carries out the programming instructions contained in it. While this is happening, the instrument can accept an additional 64 characters of data over the bus; if more are sent, the bus will hang until the microprocessor completes a scan and accepts the next 64 character string. Whenever the microprocessor finishes scanning a string, it puts a display on the front panel which reflects the state of input processing at that point. If the EOI line is asserted while sending a character to the 859, the currently programmed terminator character will be put into the input string following the character with the EOI.

To read a message from the 859, first send the talk address (with ATN on) over the bus. The instrument will then send the message currently selected by the Talk Message Select (%T) setting. The last character of this message will be the currently programmed terminator character with the EOI line asserted.

3.11.4 Talker

%T followed by its code sets the particular type of status message sent by the 859 when asked to talk on the GPIB. The codes may be 0 through 6 as follows.

0 Status of the front panel TRG'D annunciator. Its format is:

H 1 EOS or H 0 EOS

H — Designates triggered status follows.
1 — Sent if the 859 is outputting a waveform in any mode except continuous.
0 — Sent if the H 1 conditions are not true.
EOS — Terminator.

1 List of action and parameter selectors which caused programming errors. When read, this list is set to null. Its format is:

E N_1 L_1 N_2 L_2 - - - N_{12} L_{12} EOS

E — Designates error codes follow.
N_1 — A number code for 1st error type:
1 = Setting error (invalid value);
2 = Warning;
3 = Stored setting not present.
L_1 — Parameter letter of 1st setting in error.
EOS — Terminator.

2 Poll byte to be sent in response to a GPIB serial poll. Its format is:

P E EOS or P (blank) EOS

P — Designates poll type code follows.
E — Error.
(blank) — No error.
EOS — Terminator.

3 Value of the parameter in scratch pad memory selected by the most recently programmed parameter letter. Its format is:

V (Parameter) (Value) EOS

V — Designates value type code follows.
(Parameter) — Parameter name (as it would appear on front panel display when parameter key is pressed).
(Value) — Value in scratch pad memory for the designated parameter.
EOS — Terminator.

4 State of waveform parameters common to both channels. Its format is:

F(value)B(value)K(value)S(value)
W(value)R(value)EOS

5 State of waveform parameters in channel 1. Its format is:

A(value)D(value)L(value)N(value)
O(value)V(value)U(value)EOS

6 State of waveform parameters in channel 2. It format is identical to that of code 5.

Code 4 through 6 parameter letters and values are in the form of an 859 programming string. This allows the messages to be sent back unaltered to the 859 in order to set the parameters to the values they had when the messages were read.

3.11.5 Service Request Enable

%Q followed by its code selects the conditions under which the GPIB SRQ signal will be sent by the 859. The codes are:

0 SRQ not sent.

1 SRQ sent if a programming error occurred.

2 SRQ sent upon completion of a waveform output in any mode except continuous.

3 SRQ sent if either event 1 or 2 occurs.

3.11.6 End of String or Terminator Specification

%X followed by its argument designates a new End Of String (EOS) or terminator character. The argument is the decimal value of the ASCII character that is to be the new terminator: an EOS character recognized by the 859. Any ASCII character except NUL is accepted.

The terminator character has two uses. During output, it is appended to the end of every response to a talk request on the GPIB. During input, it signals the end of a group of programming characters. Since it is always recognized, even in a quoted string, it can be used to insure that the instrument is in a known state, so that following programming characters will be interpreted correctly.

At power on time, the EOS character is the line feed control character, ASCII character LF (10_{10}). When the 859 issues a talk message, the EOS character is the last byte sent. In addition, the End Or Identify (EOI) line is pulled low (END message) during the EOS character transmission. If the GPIB controller does not look for the END message (EOI line low), and it does not recognize the Line Feed (LF) as a string terminator, a new EOS character will be needed. For example, to change the EOS character from an LF to a Carriage Return (CR), program a %X13.

3.11.7 GET Mode

%G followed by its code selects what actions occur when a Group Execute Trigger (GET) command is sent to the 859. The code may be 0, 1 or −1.

0 Upon receipt of GET, the programmed waveform values are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is not continuous. This is the same sequence of events that would occur if an execute, then a trigger action (IJ) were programmed, except that no error checking is done.

1 Upon receipt of GET, the stored setting next in sequence after the last stored setting accessed is recalled if it exists. Then the actions described for code 0 are performed. This is the same sequence of events that would occur if a next setting, an execute and a trigger action (TIJ) were programmed, except that no error checking is done.

−1 Upon receipt of GET, the stored setting previous in sequence before the last stored setting accessed is recalled if it exists. Then the actions described for code 0 are performed. This is the same sequence of events that would occur if a previous setting, an execute and a trigger action (XIJ) were programmed, except that no error checking is done.

3.11.8 Return To Local

Pressing the front panel RTN LOCAL key switches the GPIB interface to the local mode if it is not in the local lockout mode. The REM (Remote) LED on the GPIB

annunciator will go off when this key is pressed. This allows manual intervention in sequences of GPIB programming. If it is desired to totally prevent front panel alteration of the instrument's state, the GPIB interface must be put into the local lockout mode (refer to paragraph 3.11.2.4, item 4).

3.11.9 Display

The single quote character (') is used to cause a string of characters to be displayed on the front panel display. This is accomplished by first programming a single quote, then the characters to be displayed, followed either by another single quote or by the terminator character. When the second quote or the terminator is programmed, the first 16 characters programmed after the first quote are displayed on the front panel. If fewer than 16 characters are programmed, then blanks are added to fill the display.

3.12 VERNIER (↑, ↓) AND CURSOR

The front panel (only) vernier increments (↑) or decrements (↓) the value in scratch pad memory, in display memory and the value in the waveform circuits (see figure 3-3). Incrementing is continuous when the key is held down. Over and under flow to the next digit is automatic. A cursor key allows you to select the digit being incremented.

3.12.1 Vernier Cursor

The vernier cursor selects which parameter digit will be altered. The cursor automatically resides between the last digit and the unit of measure. When the cursor key is pressed, the affected digit blinks. When the cursor key is pressed again, the cursor shifts to the left from the least significant to the more significant digits. Upon reaching the most significant digit, the cursor will return to the least significant digit. After the cursor is set, the digit value may be incremented by using the appropriate vernier key.

3.12.2 Vernier

Front panel changes to parameter values (but not codes) are made by using the vernier keys. The changes affect the display, display memory, scratch pad memory and the waveform circuits (no execute is necessary) as shown in figure 3-3. The two vernier keys are used to either increase or decrease parameter values. Pressing a vernier key will begin changing the least significant digit. However, you can select the digit to be incremented with the cursor key. The incrementing vernier key (↑) increases the digit value and, after 9, there is a carry to the next most significant digit. The decrementing vernier key (↓) decreases the digit value and, after 0 is reached, borrows from the next most significant digit. The vernier will also increment stored settings and shift the command recall and type 2 error displays left and right, four characters at a time, to allow viewing the entire display.

3.13 COMMAND RECALL

The command recall (CMD RCL) key allows display of the last 36 characters received by the 859 via the GPIB and keyboard, 16 characters at a time. Groups of four characters are shifted in or out of display by use of the vernier keys.

3.14 SYSTEM ACTIONS

3.14.1 Lamp Test

The LAMP TEST key lights all 22 annunciator lamps and all 16 readout LED's. The LED's each appear as ⊠ and blink.

3.14.2 Reset

The RESET key returns the 859 waveform parameters to their power-on condition. The readout becomes "859 RESET." Significant parameter values and conditions are given in table 3-1.

3.15 CLEAR ENTRY

The CLEAR ENTRY key erases a parameter value which is being entered. The key removes the numeric digits entered after the last parameter letter entry. (Clearable entries are always prefixed by an asterisk on the display.) The display is replaced by the previous value of the parameter being programmed.

3.16 EXPONENT

E, considered a numeric, followed by up to two digits denotes the power of the times 10 multiplier; e.g., E2 or $\times 10^2$. This is the multiplier of the term preceding it; e.g., 9.99E2 = 999. Unless changed negative, each new exponent's sign is positive.

3.17 KEYBOARD/DISPLAY

Keyboard controls are listed in tables 3-3 and 3-4. Readouts for key functions are listed in table 3-10.

Readout is in two slightly different modes; for example, when FREQ, DELAY and UPPER LEVEL keys are pressed, as for an inquiry as to status, the units of measure kHz, mV, nSec, etc., are seen, whereas, when the operator starts keying in the parameter value, no unit of measure is displayed. Display for coded parameters, when MODE, FUNC and TRIG FORMT keys are pressed, shows their programmed code in parentheses. An asterisk to the left of the displayed parameter name indicates that the information is in display memory only (see figure 3-3) and can be completed, erased with the CLEAR ENTRY key, terminated with an alpha key which transfers the value to scratch pad memory, or terminated with the EXEC key which transfers the value to scratch pad memory and the waveform circuits.

Table 3-10. Keyboard/Display

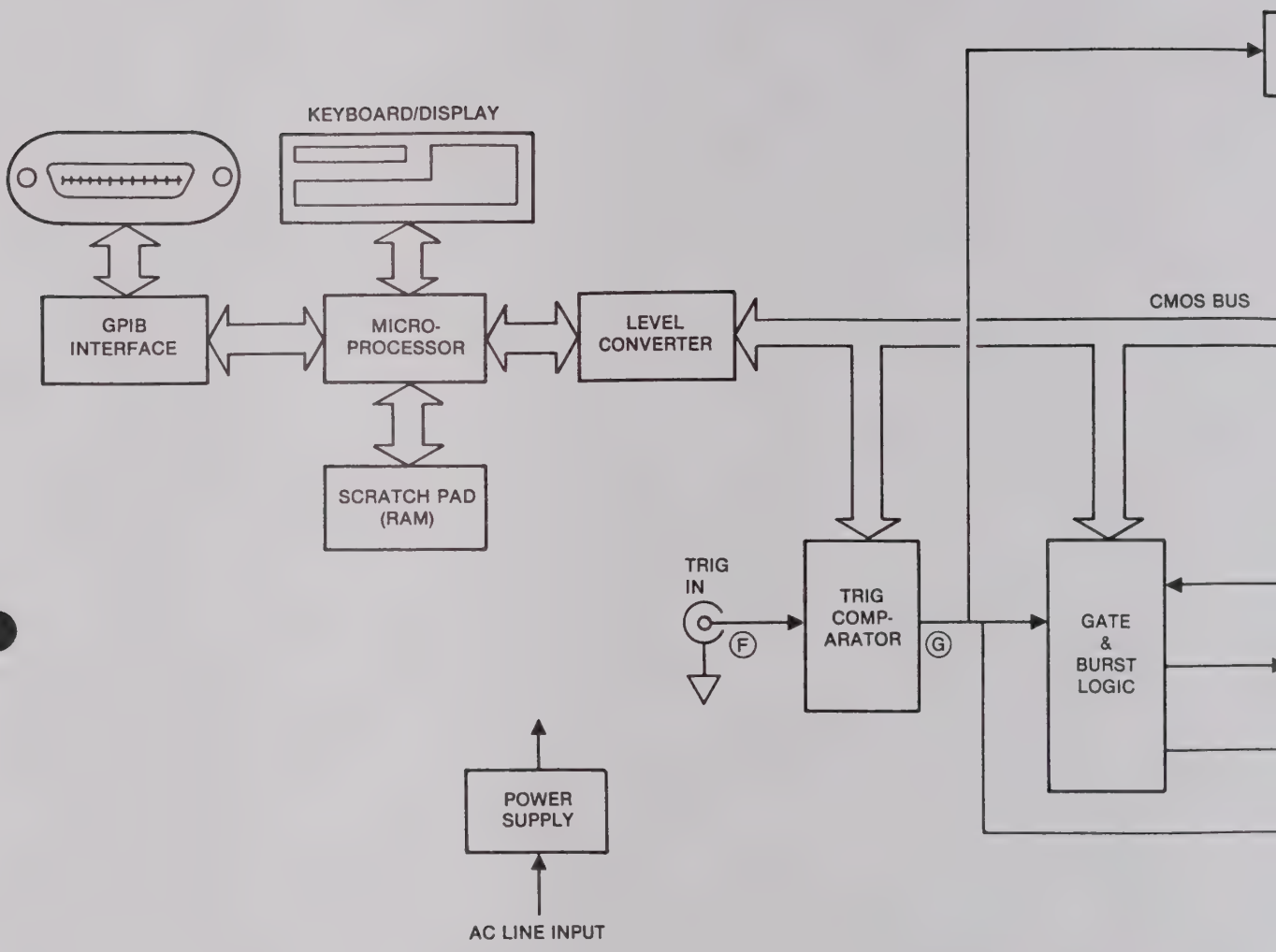
Key	Readout
ADRS	GPIB ADDR (Decimal Address)(Listen Character)(Talk Character)
BURST	BURST COUNT (Number)
CHNL	CHNL (1 or 2) SELECTED
CLEAR ENTRY	(Normal readout of previous keyed parameter)
CMD RCL	(String of letters and numbers up to 16 characters long)
CURSR	(If a value is being displayed, a digit of it blinks. If no value is being displayed, there is no effect.)
DELAY	DELAY (Value) nSec, μSec, or mSec
EXEC	EXECUTE (If no type 2 errors) ERR (error code) (error code)...(If there were type 2 errors)
EXP	(If previous display was a value or a code, it is suffixed with an E)
FREQ	FREQ (Value) mHz, Hz, kHz or MHz
FUNC	FUNC (SINGLE [0], DOUBLE [1], SQUARE [2] or INHIBIT [3])
LAMP TEST	(22 annunciator lamps and 16 readout LED's light and blink)
LEVEL LOWER	LOWR AMPL (Value) mV or V
LEVEL UPPER	UPPR AMPL (Value) mV or V
LEAD EDGE	LD EDGE (Value) nSec, μsec or mSec

Table 3-10. Keyboard/Display (Continued)

Key	Readout
TRAIL EDGE	TR EDGE (Value) nSec, μSec or mSec
MODE	MODE (CONT [0], TRIG [1], GATED [2], BURST [3], EXT WDTH [4] or TIME INT [5])
MAN TRIG	(When pressed: No display if in continuous mode, TRIGGER if in trigger, burst, or time interval mode or GATE ON if in gated or external width mode. When released: Nothing changes if in continuous, trigger, burst or time interval mode. GATE OFF if in gated or external width mode.)
NORM/COMP	NORMAL [1] or COMPLEMENT [0]
OFF/ON	OUTPUT (ON [1] or OFF [0])
PER	PERIOD (Value) nSec, μSec, mSec or Sec
+/−	− (or blank indicates +)
RCL SET	NR. (Number) RECALLED
RESET	859 RESET
RTN LOCAL	(No display)
STORE SET	SETNG (Number) STORED (if no type 2 error). ERR (error code)(error code)...(if type 2 errors)
TIME INTVL	TI INT (Value) nSec, μSec, mSec or Sec
TRIG FORMT	SLOPE RISING [0], SLOPE FALLING [1] or MAN TRIGGER [2]
WIDTH	WIDTH (Value) nSec, μSec or mSec
VERNIER ↑	(If previous display was a value or a storage location number, it is incremented. If it was a command recall or type 2 error display, the display is shifted 4 characters left.)
VERNIER ↓	(If previous display was a value or a storage location number, it is decremented. If it was a command recall or type 2 error display, the display is shifted 4 characters right.)
(Number Keys)	(The number corresponding to the key)

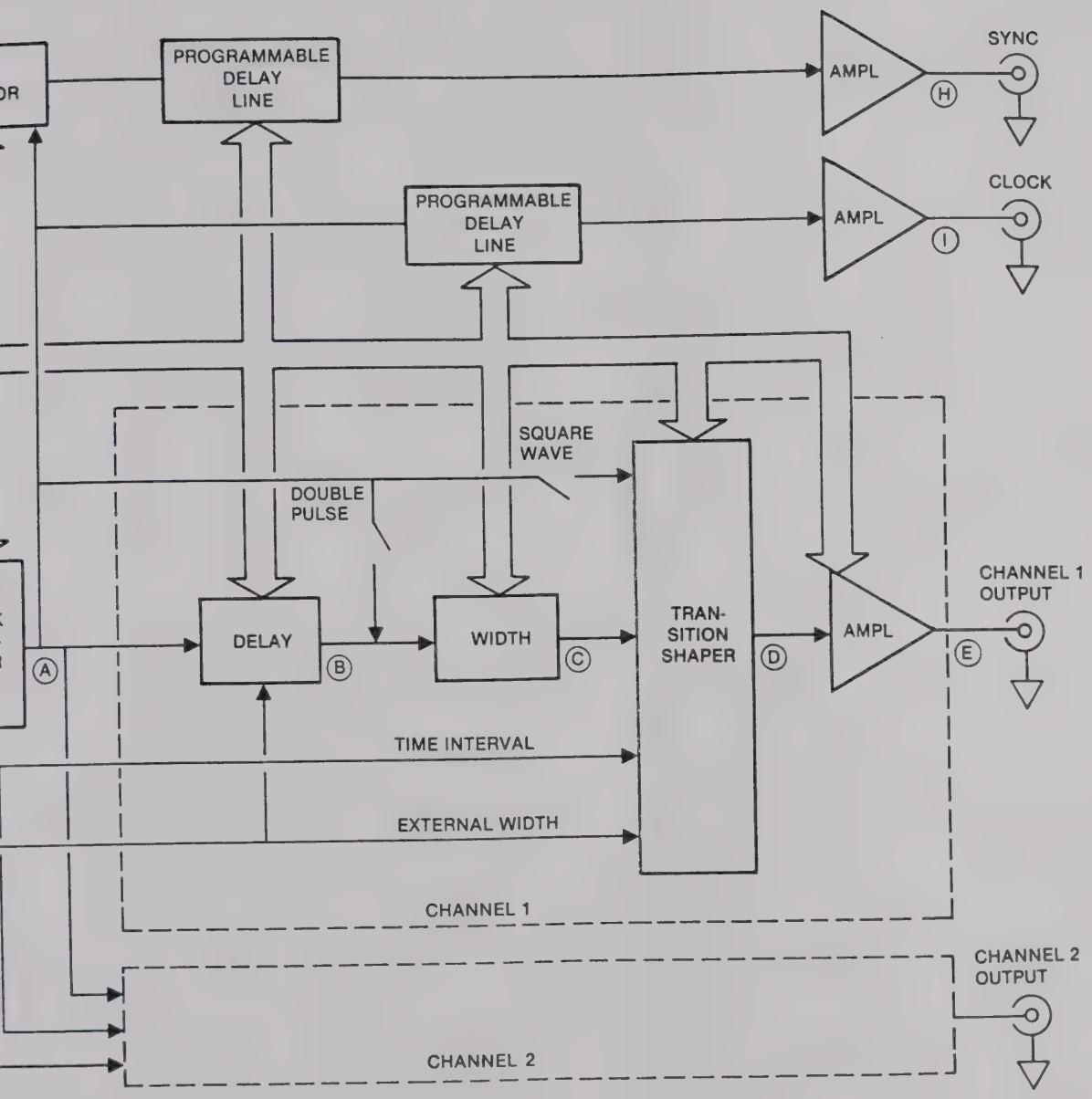
3.18 RAM BATTERIES

Batteries retain the stored settings after power is turned off. If power is off for a full 30 days, a 15 hour recharging period is required. Batteries which are fully discharged require 45 hours to receive full charge. Instrument power must be turned on to recharge the batteries. Just plugging in the 859 is not sufficient.



NOTE: Letter keys refer to figures 4-2 and 4-3.

Figure 4-1. Overall Block Diagram


PROGRAMMABLE DELAY LINE
AMPL
SYNC
H
PROGRAMMABLE DELAY LINE
AMPL
CLOCK
I
SQUARE WAVE
DOUBLE PULSE
DELAY
WIDTH
TRAN-SITION SHAPER
AMPL
CHANNEL 1 OUTPUT
A
B
C
D
E
TIME INTERVAL
EXTERNAL WIDTH
CHANNEL 1
CHANNEL 2 OUTPUT
CHANNEL 2

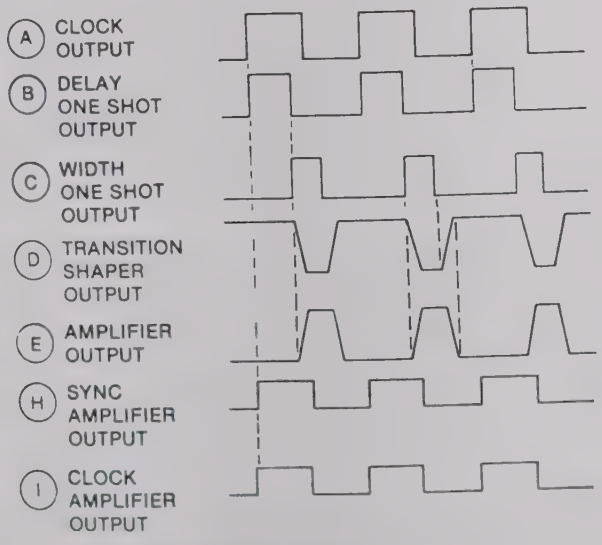
SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The major components of the Model 859 are shown in figure 4-1. Each circuit is explained in subsequent paragraphs.

The 859 has two basic sections; operational and control. The main operational circuits consist of the clock oscillator, delay and width one shots, transistion shaper, output amplifier and power supplies. Associated with the above main operational circuits are the trigger, gate and burst circuits. External outputs are the main channel outputs and the sync and clock amplifier outputs.

The microprocessor is the controller of the 859, controlling the flow of data supplied by the keyboard and General Purpose Interface Bus (GPIB). Data is processed by the microprocessor and sent on the CMOS bus to the circuit sections. Display information and GPIB messages are also controlled by the microprocessor.



NOTE: Letter keys refer to figure 4-1.

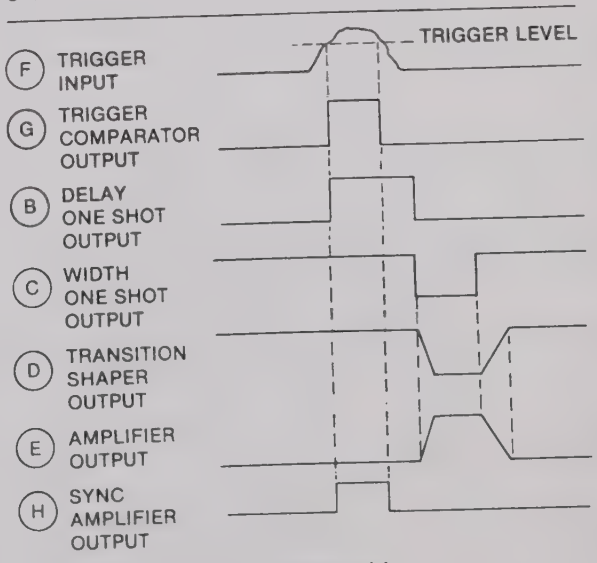
Figure 4-2. Signal Timing Diagram Continuous Mode

Pulse timing is shown in figures 4-2 and 4-3.

Each operational mode requires different connections of the circuit blocks. The connections are discussed in section 3.7:

Mode	Paragraph
Continuous	3.7.1
Triggered	3.7.2
Gate	3.7.3
Burst	3.7.4
External Width	3.7.5
Time Interval	3.7.6

Circuit connections for the functions (single pulse, double pulse and square wave) are shown in figure 3-4.



NOTE: Letter keys refer to figure 4-1.

Figure 4-3. Signal Timing Diagram, Trigger Mode

4.2 CLOCK OSCILLATOR

The interconnecting blocks within the clock oscillator circuit block are shown in figure 4-4.

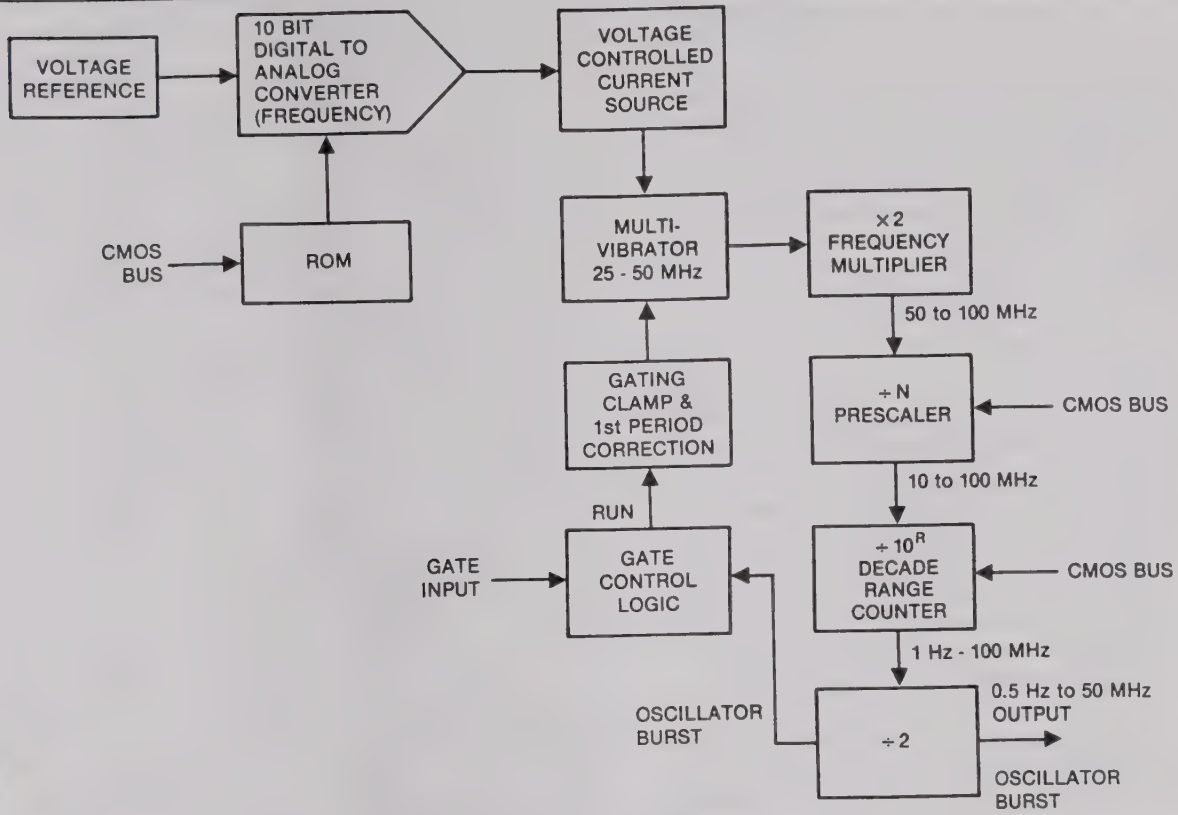


Figure 4-4. Clock Oscillator

The clock oscillator is the internal repetition rate generator that provides a train of pulses used in the continuous, gate and burst modes and provides a time base for the time interval mode. Repetition rate data is entered from either the front panel keyboard or the GPIB and routed to the microprocessor, which supplies control data to circuits in the clock oscillator block.

Basically, the clock oscillator is a voltage controlled multivibrator operating between 25 MHz and 50 MHz and a series of frequency multipliers and dividers.

Frequency control is accomplished by controlling the charging and discharging current of the multivibrator timing capacitor.

Frequency data from the CMOS bus is converted by the ROM and a 10 bit Digital to Analog Converter (DAC) to a voltage level, controlling the Voltage Controlled Current Source (VCCS).

The clock multivibrator is implemented using an ECL gate with complementary outputs. A simplified diagram is shown in figure 4-5.

The frequency of the oscillator circuit is determined by the timing capacitor C and the voltage controlled current source. The VCCS provides two tracking current sources having values of I and 2I, used for charging and discharging the multivibrator timing capacitor.

Diode D1 and D2 are current switches controlling charging and discharging of the timing capacitor. When B is high, D1 is reverse biased and D2 forward biased. The discharging current source 2I is disconnected, therefore, the total charging current is I. Once the timing capacitor has charged above the threshold, the ECL gate switches and B goes low.

D2 is reverse biased and D1 forward biased connecting the 2I discharging current source. Since the I charging current source is always connected to the timing capacitor the total discharging is $I - 2I = -I$. Thus currents charging and discharging the timing capacitor are always equal providing a symmetrical square wave from the multivibrator.

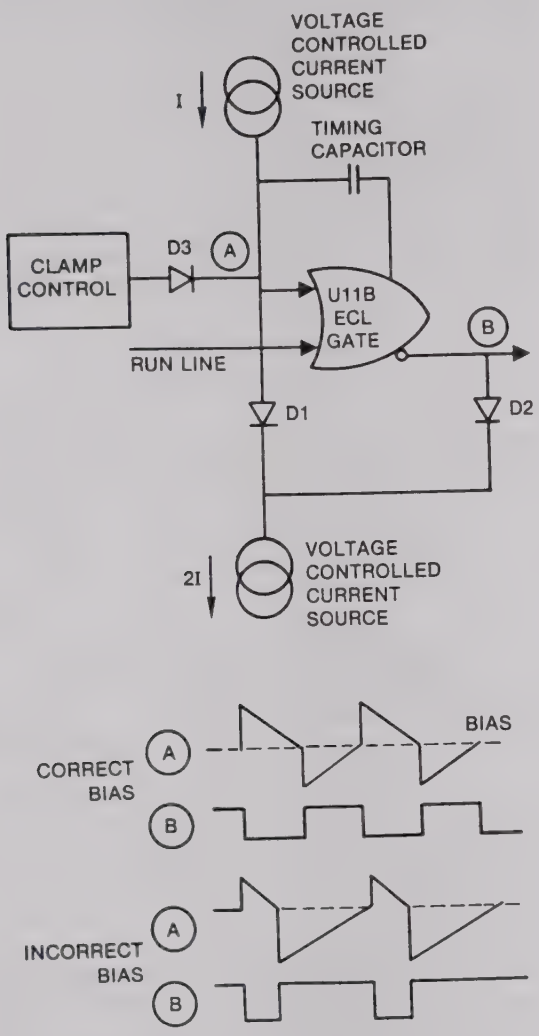


Figure 4-5. Clock Multivibrator

When the oscillator is enabled (running), diode D3 is reverse biased (run line is low). When the oscillator is disabled (stopped), diode D3 is forward biased (run line is high). Diode D3, controlled by the clamp control, clamps the oscillator input A at a specific level. The clamp level is adjusted to produce a time symmetrical first period when the oscillator is enabled.

Some nonlinearities occur in the 25 to 50 MHz multivibrator. To correct for the nonlinearity a ROM is added in the frequency controlling circuit. Frequency data from the CMOS bus provides "Addresses" for the ROM, while the ROM output data, "words," are used as data bits for the 10 bit DAC. The ROM can be programmed to increase or decrease the VCCS, thus affecting the multivibrator frequency, linearizing the multivibrator frequency.

The multivibrator free runs, in the continuous mode, driving a series of frequency multipliers and dividers. See figure 4-4. The frequency is first doubled by a $\times 2$ fixed multiplier. Then the doubled frequency is divided by $\div$ N prescaler in steps of 1,2,4,5 or 10. The divided frequency drives the $\div 10^R$ decade range counter, dividing the frequency in increments of 1, 10, 100, 1,000, 10,000, 100,000, 1,000,000 or 10,000,000. The divided frequency drives a $\div$ 2 flip flop; providing a square wave output.

An example (see figure 4-6) shows how the divider/muliplier functions. A frequency of 125 Hz is entered on the keyboard. The microprocessor controlled CMOS bus supplies data for the frequency control section (ROM, DAC, and VCCS), the $\div$ N prescaler, and the $\div 10^R$ decade range counter. The multivibrator output is programmed to 50 MHz, prescaler to N = 4 and the 10^R range counter to R = 5. The 50 MHz is doubled by the $\times 2$ multiplier to 100 MHz (50 MHz $\times 2$ = 100 MHz). The doubled frequency (100 MHz) is divided by the prescaler to 25 MHz (100 MHz $\div$ 4 = 25 MHz). The decade range counter further divides the frequency by 10^5 or 100,000 to 250 Hz (25,000,000 $\div$ 100,000 = 250 Hz). 250 Hz is divided by the $\div$ 2 flip flop producing a 125 Hz square wave.

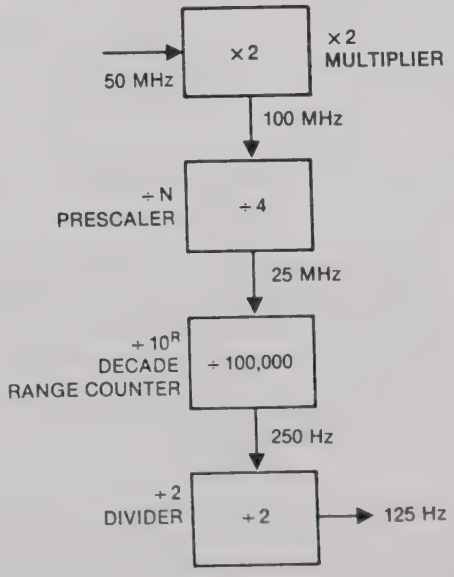


Figure 4-6. Divider and Multiplier Example

In either gate, burst or time interval modes, the multivibrator is controlled by the gate and burst control logic.

The gate input is controlled by the trigger comparator for the gate mode (paragraph 4.6) or the burst counter for burst and time interval modes (paragraph 4.7). The gate input line goes high enabling the multivibrator for the duration of the trigger signal. The output is synchronous with the trigger signal and always concludes with the complete pulse cycle (see figure 4-7).

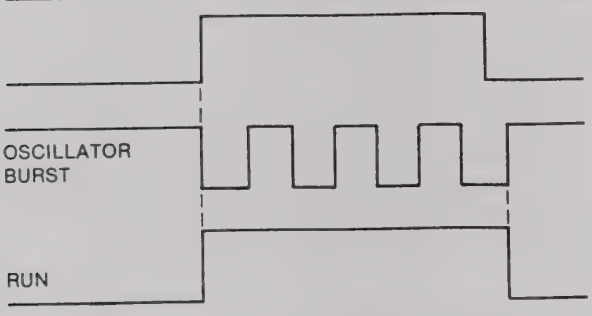


Figure 4-7. Clock Oscillator Gating

4.3 DELAY AND WIDTH ONE SHOTS

In the 859, digital one shots are used to delay pulses, relative to sync output, and to vary pulse width. As the one shots are digital they are easily controlled via the microprocessor controlled CMOS bus.

Both the delay and width one shots are similar; the circuits description deals with the common circuitry. The difference is the triggering edge of the input pulse. The delay one shot triggers on the leading edge while the width one shot triggers on the trailing edge. Signal flow and timing are shown in figures 4-8 and 4-9.

The one shot time interval is determined by a 50 MHz time base (a temperature corrrected delay line oscillator) with a series of microprocessor controlled counters and delay line.

A flip-flop controls the oscillator. A start pulse (see figure 4-8) sets the flip-flop enabling the oscillator gate input. After the oscillator pulse is delayed through the counters and delay line, the flip-flop is reset disabling the oscillator. The oscillator gate line being the one shot output.

A simplified diagram of the oscillator is shown in figure 4-10. When enabled by the control flip-flop (gate control line goes low) the circuit will oscillate with a

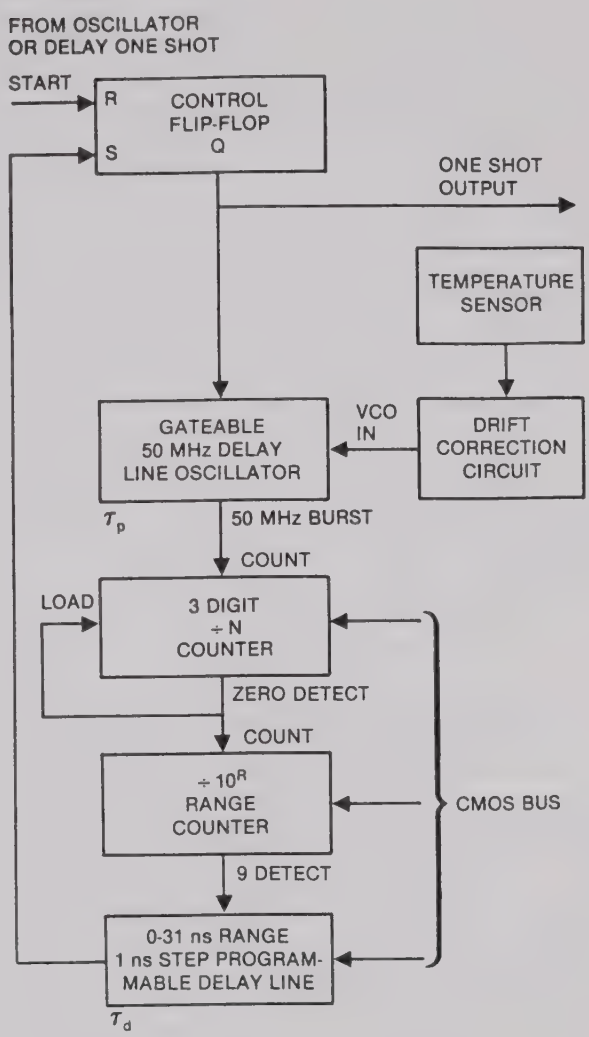


Figure 4-8. Delay & Width One Shot

20 ns period, which is determined by the 7 ns delay line, gate delays and a variable capacitor. To minimize temperature caused frequency drift, a sensor monitors the oscillator circuit temperature and controls the drift correction circuit which makes slight corrections, via a varactor diode, to the oscillator. The oscillator output drives the count line for the 3 digit ÷ N counter (figure 4-9).

The count "N" is programmed from the CMOS bus. When the counter receives the first positive transition, the data, N, is loaded into the counter. Each clock pulse decrements the count by one. Upon reaching the last count (zero) the zero detect line (counter output) goes low, providing an input pulse for the decade

range counter. The counter will continue this cycle of loading 3 digits and counting to zero until the oscillator is gated off.

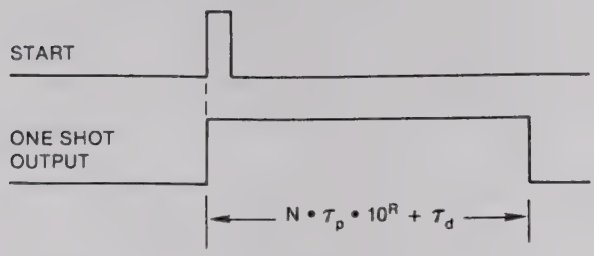


Figure 4-9. Delay and Width One Shot Timing

Data from the CMOS bus is loaded into the $\div 10^6$ (decade) range counter. The frequency is further divided in increments of 1, 10, 100, 1000 or 10,000. The counter output (9 detect line). Drives the programmable delay line.

The programmable delay line delays the pulse from 0 ns to 31 ns in 1 ns steps. Figure 4-11 shows a simplified diagram for the programmable delay line. One or all of 5 delay line sections may be switched in depending on the delay programmed. Delay lines are in steps of 1 ns, 2 ns, 4 ns, 8 ns and 16 ns. Delays line sections are additive allowing programming in 1 ns steps: for example, 1 ns + 2 ns + 8 ns = 11 ns.

To explain the time relationship in the one shot, the following formula is used (figure 4-9):

Time Interval = $N T_p 10^R + T_d$.

Where

N = the programmed 3 digits.
T_p = the period of the oscillator (20 ns)
10^R = the programmed decade range
T_d = the programmed delay line period

For example,

N = 051
T_p = 20 ns
10^R = 10
T_d = 15 ns

Therefore,

(051 × 20 ns × 10) + 15 ns =
10,200 ns + 15 ns = 10,215 ns total delay within the one shot.

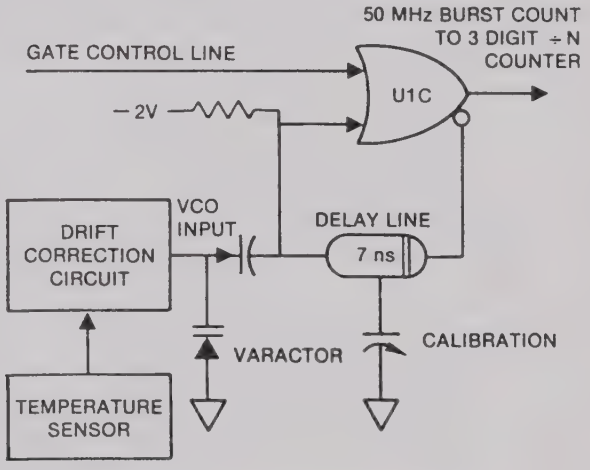
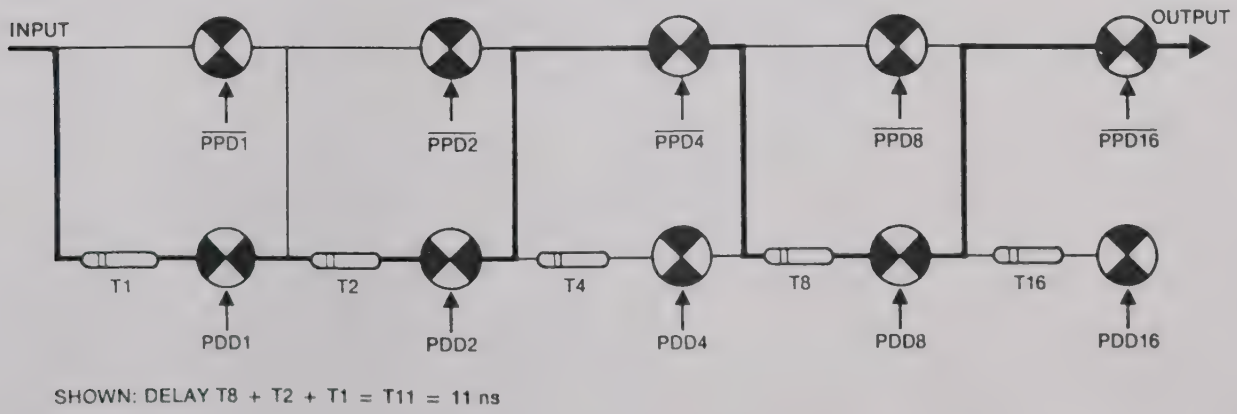


Figure 4-10. Delay Line Oscillator



SHOWN: DELAY T8 + T2 + T1 = T11 = 11 ns

Figure 4-11. Programmable Delay Line

4.4 TRANSITION SHAPER

The transition shaper shapes the pulse leading edge and the trailing edge and provides initial signal level control. Microprocessor control allows the amplitudes to be increased or decreased without effecting the programmed transition times. The circuit blocks for the transition shaper are shown in figure 4-12 and circuit operation is discussed in the following paragraphs.

The basic reference for the transition shaper is the voltage V_u. V_u is generated by a CMOS bus controlled amplitude DAC and a voltage reference. V_u is programmed between 0.8V and 2.0V.

V_u provides the reference input to the leading and trailing edge DACs. Each edge DAC controls a pair of tracking Voltage Controlled Current Sources (VCCS). The leading edge DAC controlls the positive current source and the trailing edge DAC controlls the negative current source.

The leading edge to trailing edge time ratio cannot exceed 50:1. The actual ratio is dependent on the current sources. The transition range is determined by a of capacitor selected by the microprocessor.

All main output signals of a channel are processed by the transition shaper regardless of operation mode. Logic gate U3 accepts the input signal and its output drives a current (electronic) switch. When U3 output goes high the range capacitor is charged by the current from the positive VCCS $+I_1$. Leading edge transition time is determined by the current charging the range capacitor. A specific current for a specific tran-

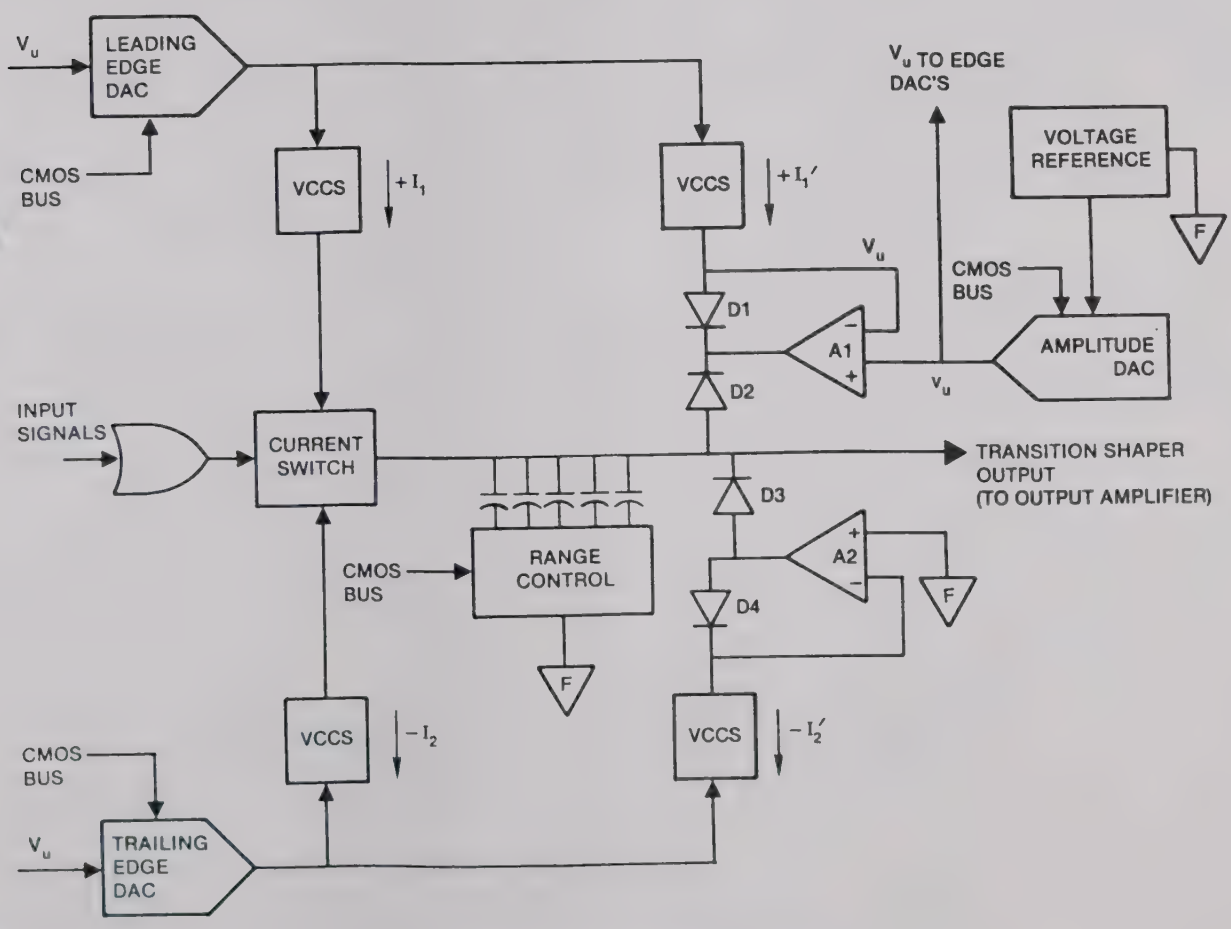


Figure 4-12. Transition Shaper

sition time is required to charge the capacitor depending on the voltage level and the range capacitor. Increasing the charging current decreases the transition time and decreasing the charging current increases the transition time. The capacitor charges to the level V_U, where it is limited by the upper level voltage clamp.

The upper level voltage clamp consists of op amp A1 and referenced to V_u', a pair of matched diodes D1 and D2 and a VCCS $+ I_1'$ tracking the charging current source. As A_1 is an op amp, the anode of D1 is at v_u. The current $+I_1'$ will flow through D1 and sink to A1. At levels less than V_u, D2 is reverse biased. When the output reaches V_u, D2 is forward biased; as D1 and D2 are matched they will have equal current ($+ 1_1$ and $+ I_1'$) flowing through them, clamping the output level to V_u.

When U3 output goes low the range capacitor is discharged by the $-I_2$ VCCS. The trailing edge transition is determined by the current discharging the range capacitor. For a specific transition time a specific current is required to discharge the capacitor, dependent on the voltage level and the range capacitor. Increasing the discharge current decreased the transition time and decreasing the charging currents increases the transition time. The range capacitor will discharge until limited by the lower level voltage clamp.

The lower level clamp is similar to the upper level clamp. The op amp A2 is referenced to F. As A2 is an op amp, the cathode of D4 is at F, current $-I'_2$ will flow from A2 through D4. At levels greater than F, diode D3 is reverse biased. When the output reaches F, D3 is forward biased; as D3 and D4 are matched they will have equal current ($-I_2$ and $-I'_2$) flowing through them, thus clamping the output level a F.

The transition shaper drives the output amplifier.

4.5 OUTPUT AMPLIFIER

The output amplifier is an inverting amplifier providing an output pulse from 40 mV to 20V p-p. Externally programmed upper and lower level values are converted by the microprocessor to the proper amplitude and offset values. The amplifier may be isolated from the 50Ω output by relay K2; see section 3.9.2. The output amplifier block diagram (figure 4-13) and the following paragraphs summarize amplifier operation.

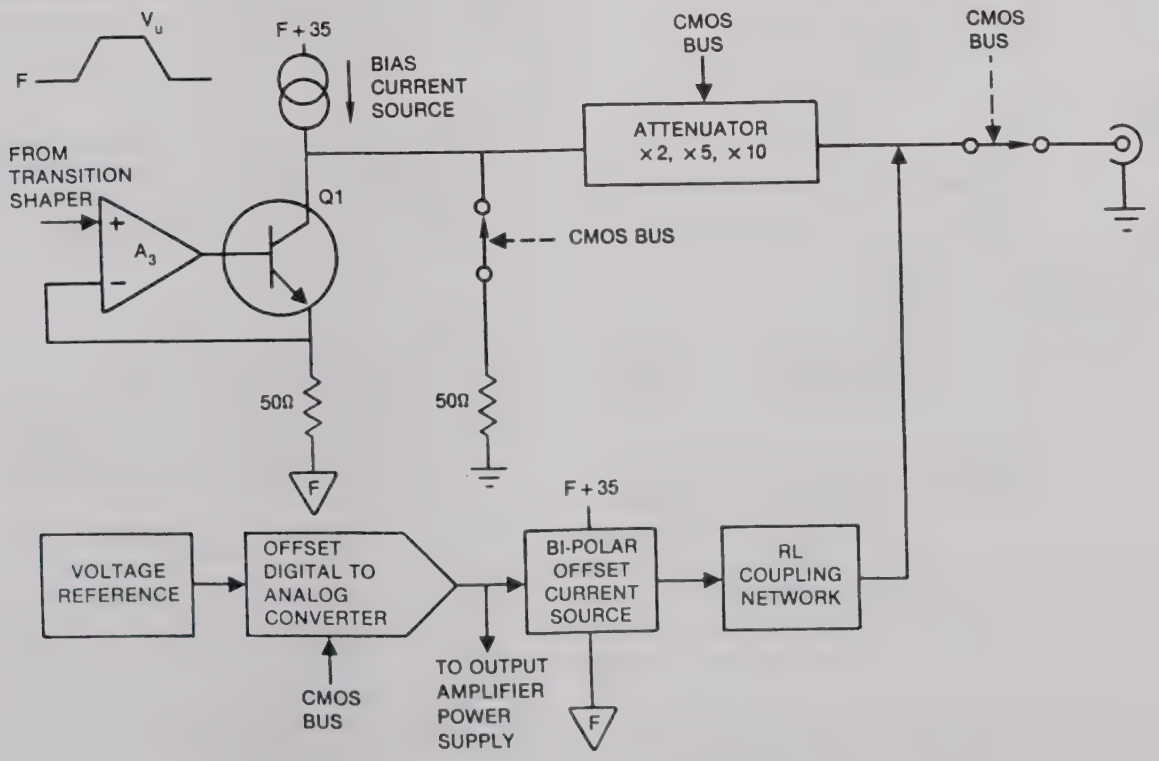


Figure 4-13. Output Amplifier

Both output amplifier and transition shaper circuit use a floating supply. Floating supplies are voltages that shift relative to circuit ground, depending on the programmed output levels, while maintaining absolute levels. The shifting of the floating supplies, based on the output level, biases Q1 to operate under its breakdown voltage and minimizes power dissipation in Q1. See paragraph 4.12 for a description of the floating supply.

The output signal from the transition shaper is applied to the positive (non-inverting) input of the FET amplifier A3. The output of A3 drives Q1. Together, A3 and Q1 comprise the amplifier portion of the output amplifier. The amplifier produces negative pulses, as F, a controlled voltage level, is always negative with respect to ground. To produce positive pulses the input to A3 must be complemented and a positive offset summed with the pulse amplitude. A current source biases the output amplifier to an optimum level, between F +35 and F, keeping the output amplifier operating in the active region.

A microprocessor controlled relay K1 switches the 50Ω backmatch resistor in or out depending on the programmed amplitudes. When the 50Ω is in, maximum output is limited; see table 1-1

The attenuator is programmable in X1, X2, X5 and X10 steps allowing attenuation steps from X1 to X100 and attenuated output levels down to 40 mV. Specified resolution in signal level is obtained by a combination of input signal level control, amplifier gain, and output attenuation.

Offset control is accomplished by summing a bi-polar offset current source through a RL network to the output of the attenuator. The offset value is controlled by the 10 bit offset DAC, which is programmed by the microprocessor controlled CMOS bus.

4.6 TRIGGER COMPARATOR

The trigger comparator receives, processes and distributes the trigger signal to the appropriate circuit blocks. The intraconnection of the trigger comparator circuit block is shown in figure 4-14. (A front panel annunciator indicates the occurence of a triggered output).

The input signal is processed by a high speed schmitt trigger to derive a fast rise time signal from random

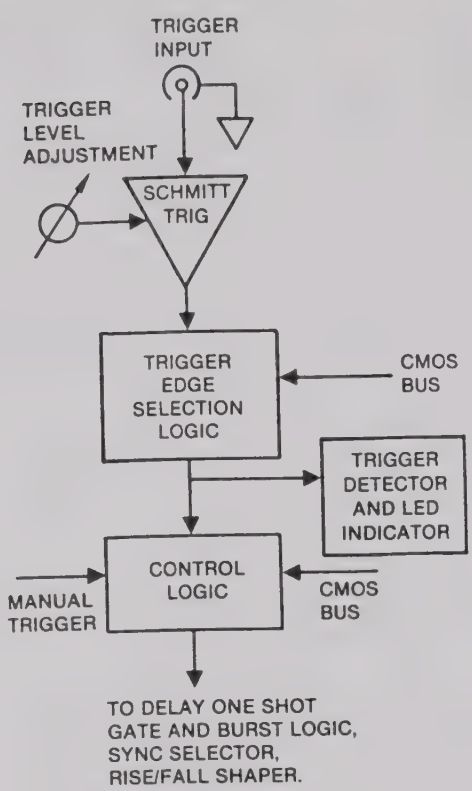


Figure 4-14. Trigger Comparator

slope input signals. The dc trigger level is summed with the input signal, allowing the input trigger point to be adjusted between −5V and +5V. Increasing the dc voltage increases the required signal voltage that will be accepted as a trigger.

The trigger format logic, externally programmed by the keyboard or GPIB, selects the phase or slope on which the 859 will trigger.

The control logic circuit selects the external trigger, manual trigger or no trigger at all, depending upon the programmed mode of operation.

The trigger detector senses transitions at the output of the edge logic and flashes an LED. The LED flashes for 50ms for each trigger occurence. In burst, time interval and gate modes, the trigger indicator remains on until the cycle is completed.

4.7 Burst Counter

The burst counter, figures 4-15 and 4-16, controls the clock oscillator for a selected count N, during burst and time interval modes. The circuit internally functions identically for both modes, only the method of programming the oscillator and counter is different.

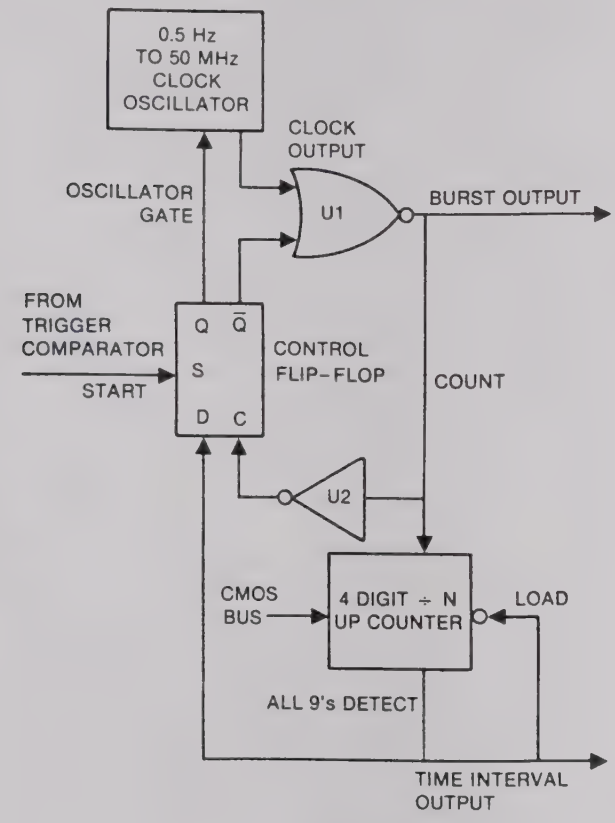


Figure 4-15. Burst Counter

The time interval is N τ_p, where N is the programmed burst count and τ_p is the programmed oscillator period. For example if $\tau_p = 1\mu s$ and N = 1000 then the time interval of the burst counter is $1\mu s \times 1000$ or 1ms.

In the time interval mode, the time interval is programmed via the keyboard or GPIB. Then the microprocessor selects both a specific burst count and an oscillator period. In the burst mode, the burst count (between 1 and 10000 pulses) and oscillator period (from 20 ns to 2s) are separately programmed via the keyboard or GPIB.

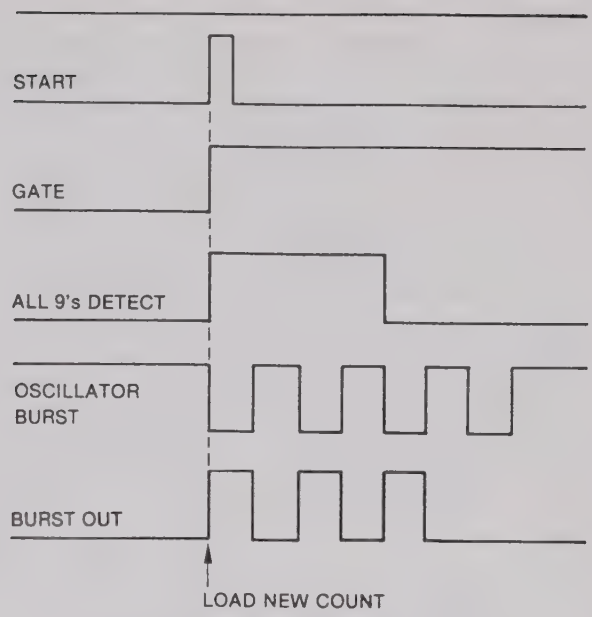


Figure 4-16. Burst Counter Timing

Once data has been entered, the burst counter operates indentically in both modes. A start pulse from the trigger comparator sets the control flip-flop enabling the oscillator gate line (Q output goes high). The Q line goes low enabling the NOR gate U1. The flip-flop D line goes high and each succeeding clock pulse (count) maintains Q high and Q low.

The first count pulse supplied to the 4 digit ÷ N programmable up counter loads the data into the counter. The data loaded is the ten's complement of N. Each successive count pulse increments the counter by one count (N + 1). Upon reaching the all nines count, the counter's nine detect line goes low controlling the D line of the control flip-flop.

The D input goes low (end of N count). Upon receiving the next triggering edge of the clock (count), Q (gate) goes low disabling the oscillator. $\bar{Q}$ goes high disabling the NOR gate U1.

To compensate for delays in disabling the clock oscillator, U1 is disabled to ensure that clock counts are not erronously output; something that could occur when operating at high clock rates.

The burst counter has two outputs, one for each mode. The burst output is driven from the count line (output of U1). The time interval output is driven by the – N counter output (nine detect).

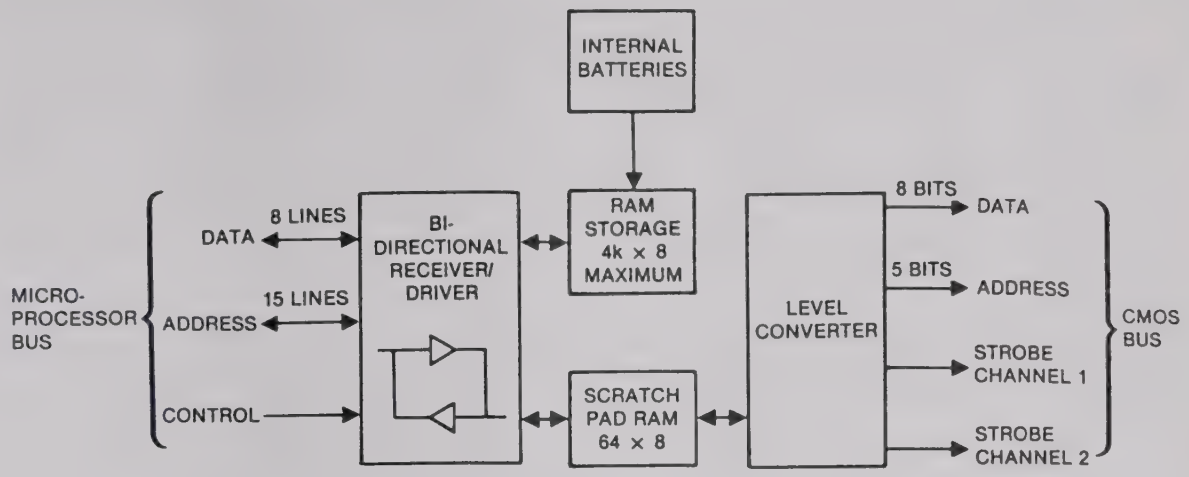


Figure 4-17. RAM

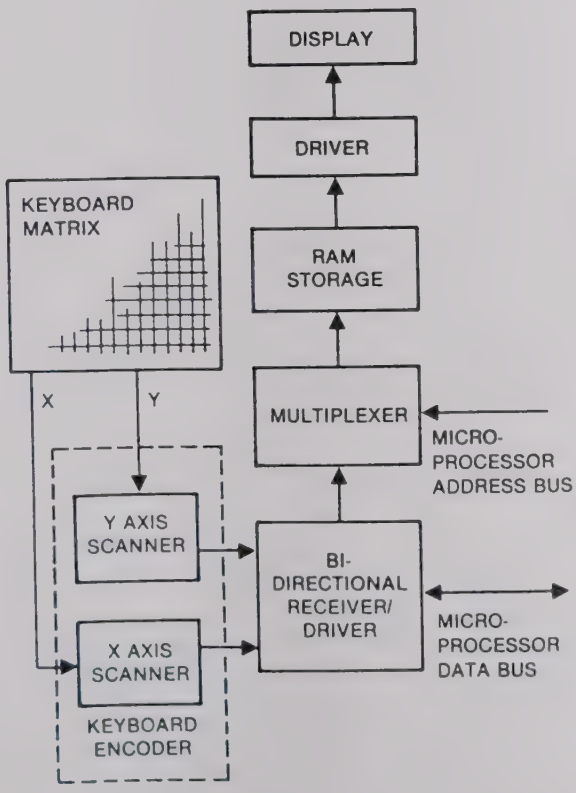


Figure 4-18. Front Panel Keyboard/Display

4.8. RAM BOARD

The RAM board contains two sets of memories, a 4k × 8 RAM for stored settings and a 64 × 8 scratch pad memory. The block diagram for the RAM board is shown in figure 4-17.

The storage RAM stores settings of parameters and values for 25 settings (standard memory) in a 1k × 8 RAM. An optional 4k × 8 RAM expands memory to a maximum of 100 stored settings. With power off data is maintained in RAM up to 30 days by use of internal batteries; see section 3.18. RAM data is buffered from the microprocessor bus by a bi-directional receiver/driver.

A 64 × 8 scratch pad RAM temporarily stores data until an execute command is received. The data is buffered from the microprocessor bus by the bi-directional receiver/driver. Data is transferred through a level converter to the CMOS bus. The CMOS bus provides addresses, data and channel strobes to the analog circuitry.

4.9 FRONT PANEL KEYBOARD/DISPLAY

The keyboard and display allow a manual method of programming the 859 and a visual indication of parameter status. A block diagram is shown in figure 4-18.

The front panel contains a 42 key keyboard, a 16 character alphanumeric LED display with 22 individual LED annunciators and the power on/off switch. The front panel assembly is connected elec-

trically to the 859 by two cables. One cable is on the power switch and can be disconnected on the rear panel. The other cable carries the keyboard and display signals and is plugged into the mother board at J18. The front panel assembly consist of three subassemblies: the keyboard, the LED display and a pc board which interfaces to the microprocessor in the 859. The microprocessor accesses the keyboard and display just as if they were read and write memory locations.

4.9.1. Keyboard

The keyboard consists of 42 printed circuit switches arranged in 6 × 8, X-Y matrix. The keyboard matrix is scanned by a keyboard encoder chip. When a contact closure is detected, the encoder stops scanning, provides a delay for contact bounce and latches a data ready strobe pulse. The microprocessor is informed by the data ready strobe that a key is pressed. The microprocessor decodes the keyboard address, strobes the keyboard encoder and reads the buffered keyboard output data. The keyboard output data is a binary number between 0 to 63 corresponding to the key pressed. The data ready strobe also triggers a 100 ms, 3 kHz audible tone each time the key is pressed. When the keyboard contact closure is released the encoder resumes scanning for the next closure.

4.9.2 Display

The display is a 16 character alphanumeric LED readout and 22 LED annunicators. The bi-directional receiver/driver receives data from the microprocessor data bus. The display data is multiplexed, held in temporary RAM storage, strobed into the display driver, and displayed on the front panel.

4.10 GENERAL PURPOSE INTERFACE

The GPIB interface (see figure 4-19) allows the instrument to be remotely programmed by a minicomputer, calculator, etc., via the General Purpose Interface Bus (GPIB). The GPIB interface is an implementation of IEEE Standard 488-1978. It supports the following 488-1978 defined interface functions: Source Handshake (SH1), Acccepter Handshake (AH1), Talker (T6), Listener (L4), Service Request (SR1), Remote Local (RL1), Device Clear (DC1) and Device Trigger (DT1). This bus transfers messages in bit parallel and byte serial fashion. The bus has 16 signal lines, and they are:

8 Data lines (DIO1 through DIO8)

5 Control lines (ATN, IFC, SRQ, EOI and REN)

3 Handshake lines (NRFD, NDAC and DAV)

These lines are defined in paragraph 3.11, as is operation with the GPIB.

The GPIB interface does the following three functions:

1. Detects the My Listen Address (MLA) and My Talk Address (MTA).

2. Does the proper listen handshake when either attention (ATN) is true, or the listen latch is set, and transfers messages when the talk latch is set.

3. Provides isolation through optical couplers.

In order to reduce the number of opto-isolators, the messages are transferred in bit serial fashion through two Universal Asynchronous Receiver/Transmitters (UART). All 16 GPIB lines are buffered and terminated through bus transceivers. The UART and status outputs are connected to the microprocessor data line via tri-state buffers.

The operation of the UART is fairly simple. Each UART consists of two independent sections called receiver and transmitter, and both of them may operate simultaneously. The UARTs are primarily used to convert parallel information into serial and serial information into parallel. The receiver receives its information in serial and converts it into an 8 bit parallel byte, whereas the transmitter converts an 8 bit parallel byte into bit serial output. The transfer rate of the serial output is determined by the clock frequency of the UART. Here the UART clock frequency is set at 1.25 MHz.

The interface completely insulates the microprocessor from GPIB and hence the microprocessor is relieved from the GPIB transactions. The microprocessor constantly monitors the status outputs from the interface and takes actions according to that. There are six status bits tied to the microprocessor data bus: Data Ready, GPIB Busy, End, Remote, Talk and Listen.

4.10.1 Data Ready

The Data Ready bit informs the microprocessor that the UART has received valid data from the GPIB. Only when this bit is true will the microprocessor read the byte from the UART.

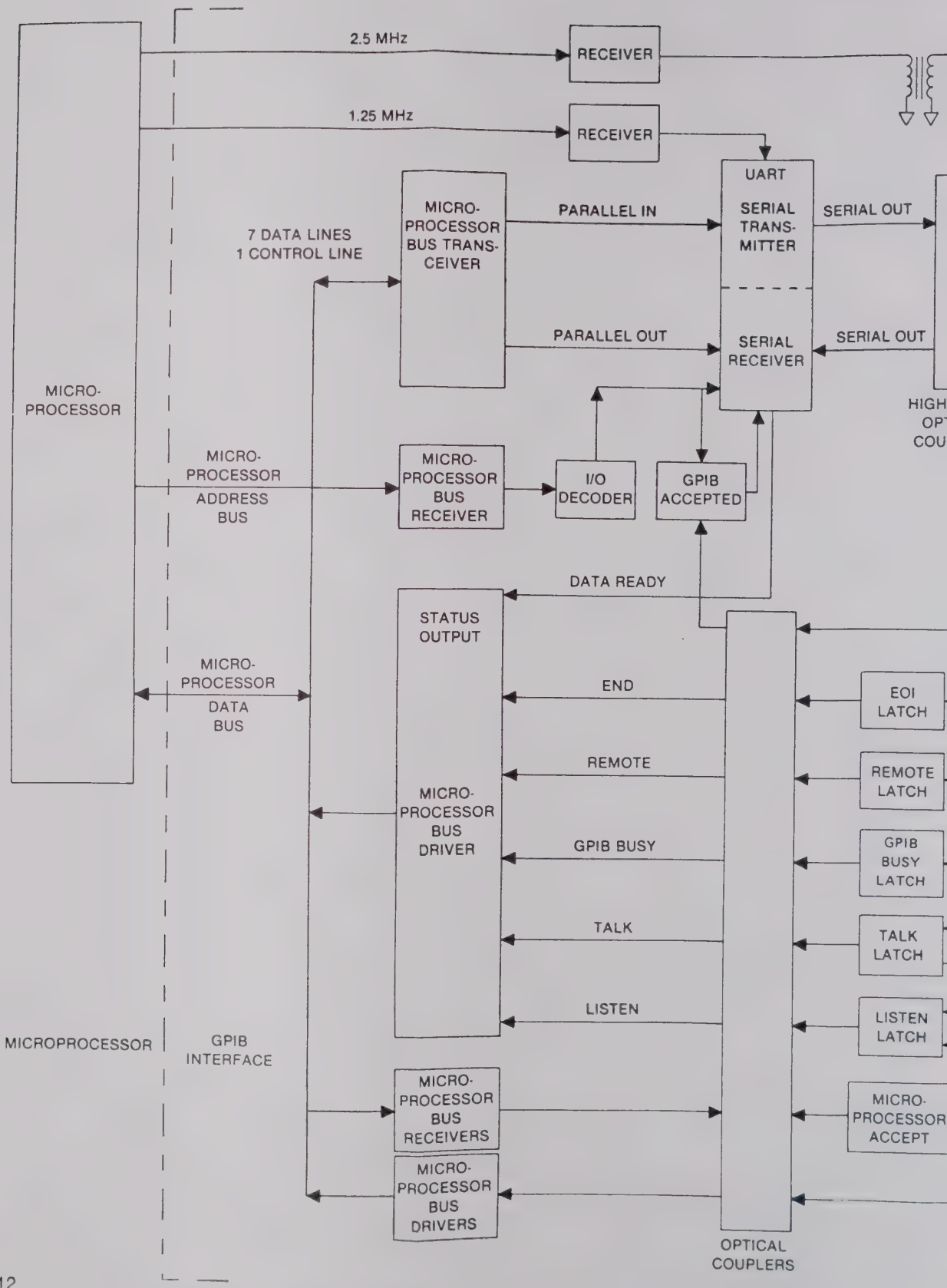
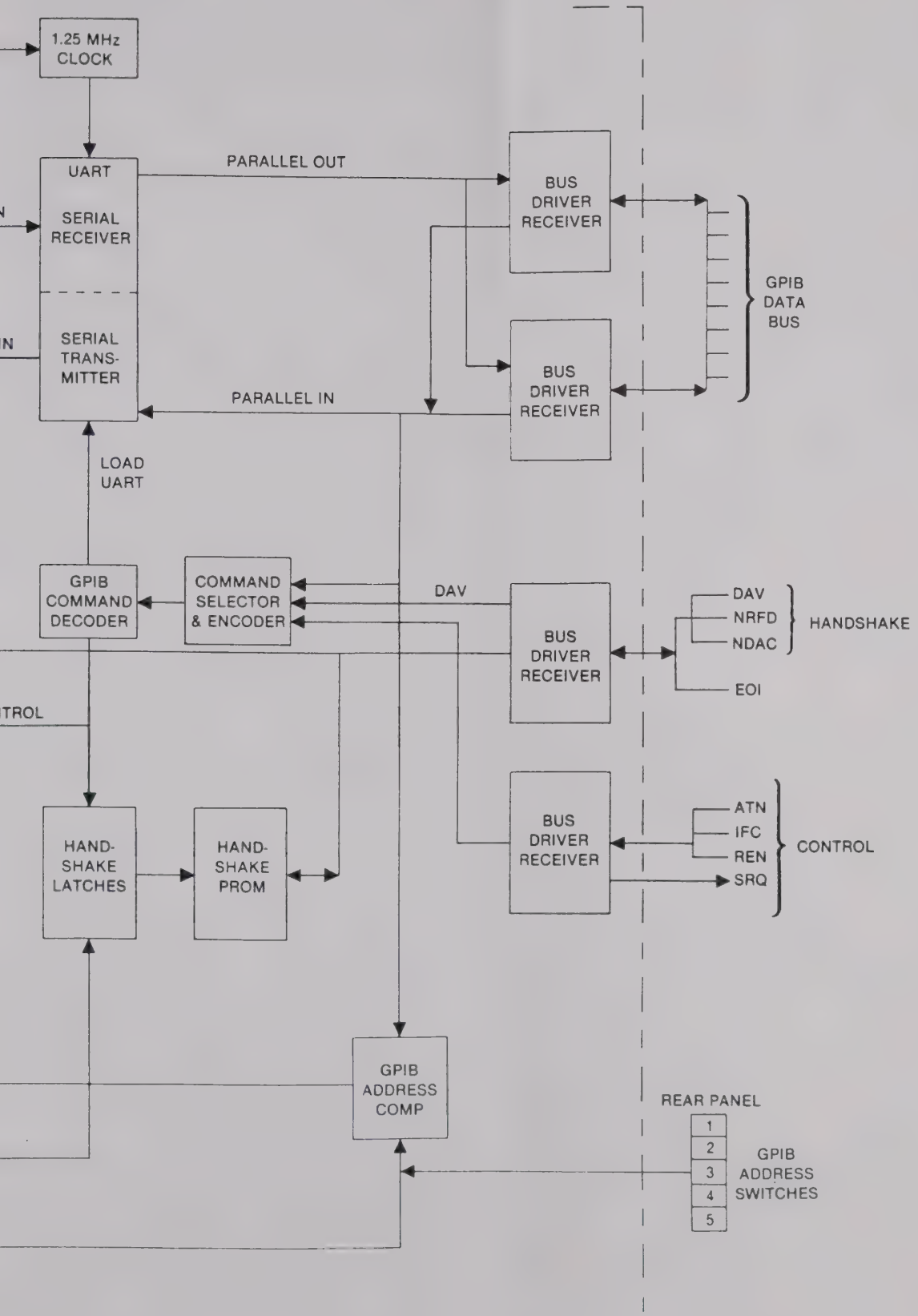


Figure 4-19. GPIB Interface


1.25 MHz CLOCK
UART
SERIAL RECEIVER
SERIAL TRANS-MITTER
PARALLEL OUT
PARALLEL IN
LOAD UART
BUS DRIVER RECEIVER
BUS DRIVER RECEIVER
GPIB DATA BUS
GPIB COMMAND DECODER
COMMAND SELECTOR & ENCODER
DAV
BUS DRIVER RECEIVER
DAV
NRFD
NDAC
HANDSHAKE
EOI
BUS DRIVER RECEIVER
ATN
IFC
REN
SRQ
CONTROL
HAND-SHAKE LATCHES
HAND-SHAKE PROM
GPIB ADDRESS COMP
REAR PANEL
1
2
3
4
5
GPIB ADDRESS SWITCHES

4.10.2 GPIB Busy

The GPIB Busy bit is used during the talk mode to find out whether GPIB has accepted the data byte sent through the UART. Any time the microprocessor wants to send a byte via GPIB, first it checks that the Talk status bit is true and then it checks that GPIB Busy status bit is false. If the GPIB Busy status is false, then the microprocessor will load a byte into the UART and cause the GPIB Busy signal to go high (true). This prevents the microprocessor from loading any more bytes into the UART. The byte loaded into the UART is transmitted serially across the optocoupler to the GPIB side of the UART. When all the 8 bits of the byte are present, the data valid (DAV) line is set low. When the listener on the GPIB senses the DAV line is low, he accepts the byte by raising the data accepted (NDAC) signal high. The NDAC signal is received and causes the GPIB Busy signal to go low (false). Once the GPIB Busy signal goes low, the microprocessor can transmit another byte in the same manner.

4.10.3 End

The End bit is monitored by the microprocessor any time it reads a byte from the UART. If this bit is true, then the microprocessor assumes that it has received the last byte of the message sequence and treats it as a terminating character.

4.10.4 Remote

The Remote bit indicates to the microprocessor whether the 859 is in remote control or local control.

4.10.5 Talk

The Talk bit will be set any time the 859 receives its assigned talk address. When the microprocessor senses this bit as true, it sends the appropriate talk message.

4.10.6 Listen

The Listen bit will be sent any time the 859 receives its assigned listen address. When the microprocessor senses this bit as true, it prepares to receive the data bytes through the UART.

4.10.7 Service Request

Service Request (SRQ) is a bit sent by the microprocessor to the GPIB when it wants to talk. The controller will eventually cause a talk status bit to be generated and allow the microprocessor to place a talk byte on the interface.

4.11 MICROPROCESOR (Microprocessor and Memory RAM Boards)

The microprocessor (see figure 4-20) acts as the central processing unit, receiving information from the GPIB, the keyboard and the 859 subsystems and acting on these inputs as dicated by the software. Software directs the processor to address the subsystems and issue commands and data which direct the 859 to output the desired signals.

Software refers to a sequence of commands executed by the internal microprocessor. This sequence of instructions stored in ROM commands the microprocessor to perform according to the 859 specification. The microprocessor is powerless without a program to run; therefore, the software is one of the most vital elements of the digital section. All information transfer takes place under the control or supervision of the software. Programs are composed of machine language instructions, messages and tables that provide sequencing information.

Program data from the ROM, temporary data from the RAM, and input data from the keyboard or GPIB are hooked up to the microprocessor through an interconnection bus on the mother board. Data from the microprocessor software is sent to the rest of the instrument via a scratch pad memory.

The two boards of the microprocessor section (microprocessor and memory RAM) receive and drive a 43 wire data bus terminated on the mother board.

4.11.1 Microprocessor Board

This board contains an eight bit processor, software in ROM, buffers, decoders and two I/O ports. Figure 4-20. shows the basic blocks of the microprocessor. Address lines are buffered to the mother board. Eight bidirectional data lines are received and driven to the mother board. Control signals necessary to describe the transaction are buffered to the mother board. Ten megahertz clock pulses are generated and buffered to the mother board.

Integrated circuit memories on ROM support the basic program in the 859 while limited RAM serves as a microprocessor scratch pad for calculations.

An I/O port generates eight control lines sent to the analog section of the instrument. These control lines are used to provide the microprocessor a facility to trigger the instrument or provide other control functions as options.

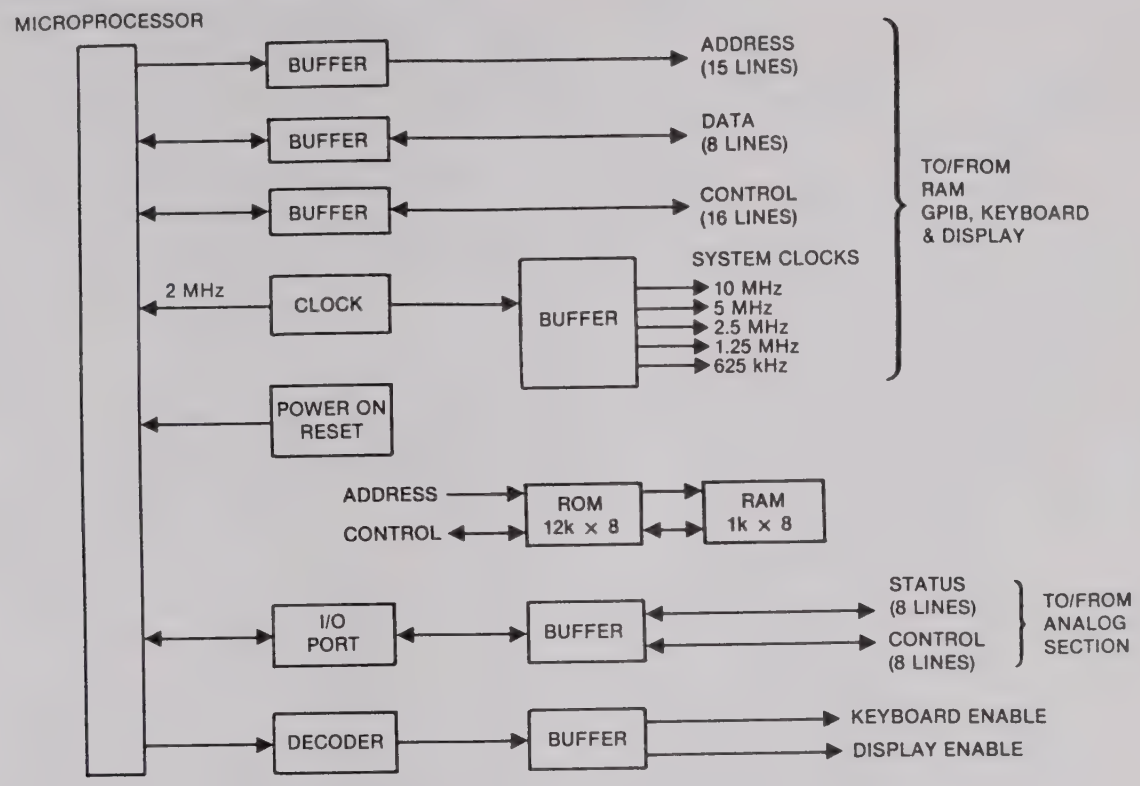


Figure 4-20. Microprocessor

Eight status lines are sent to the microprocessor to indicate that the second channel has been installed and to provide for manual triggering.

4.12 POWER SUPPLY

All 859 power supplies (figure 4-21) consist of linear regulators with capacitor input filters. Supply components are divided between the rear panel and two printed circuit boards. The transformer and high current rectifiers are located on the rear panel with all other power supply components located on two printed circuit boards.

A 2 channel 859 requires 14 separate power supplies; a single channel unit requires 10 supplies. TTL and ECL logic gates are powered by their own supplies, TTL (+ 5V) and ECL (− 2V and − 5V). The GPIB interface is powered by its 5V supply, which isolates it from the other circuitry. Also + 15V and − 15V supplies are provided primarily for the analog circuitry.

Each channel output amplifier and transition shaper requires 4 floating (F) power supplies; F + 35, F, F + 15 and F − 15. The floating supplies are voltages that shift levels relative to circuit ground, depending on programmed output levels, while maintaining absolute voltage levels of + 35V, + 15V and − 15V. The synthesized "F" ground is derived from a simple 35V regulator and controlled by the offset DAC. "F" ground may be varied between − 10V to − 30V relative to circuit ground. The floating supplies allow the output amplifier to produce a pulse of any offset and amplitude within the operating range of the 859 (see section 1.2.2.1), operate under its breakdown voltage level and to minimize power dissipation

A temperature sensor monitors the heat sink temperature. If the temperature exceeds the limit, the primary voltage is interrupted, shutting down the unit. After cooling down, the unit will power up, automatically, reset to initial power on conditions and loose any non-stored settings.

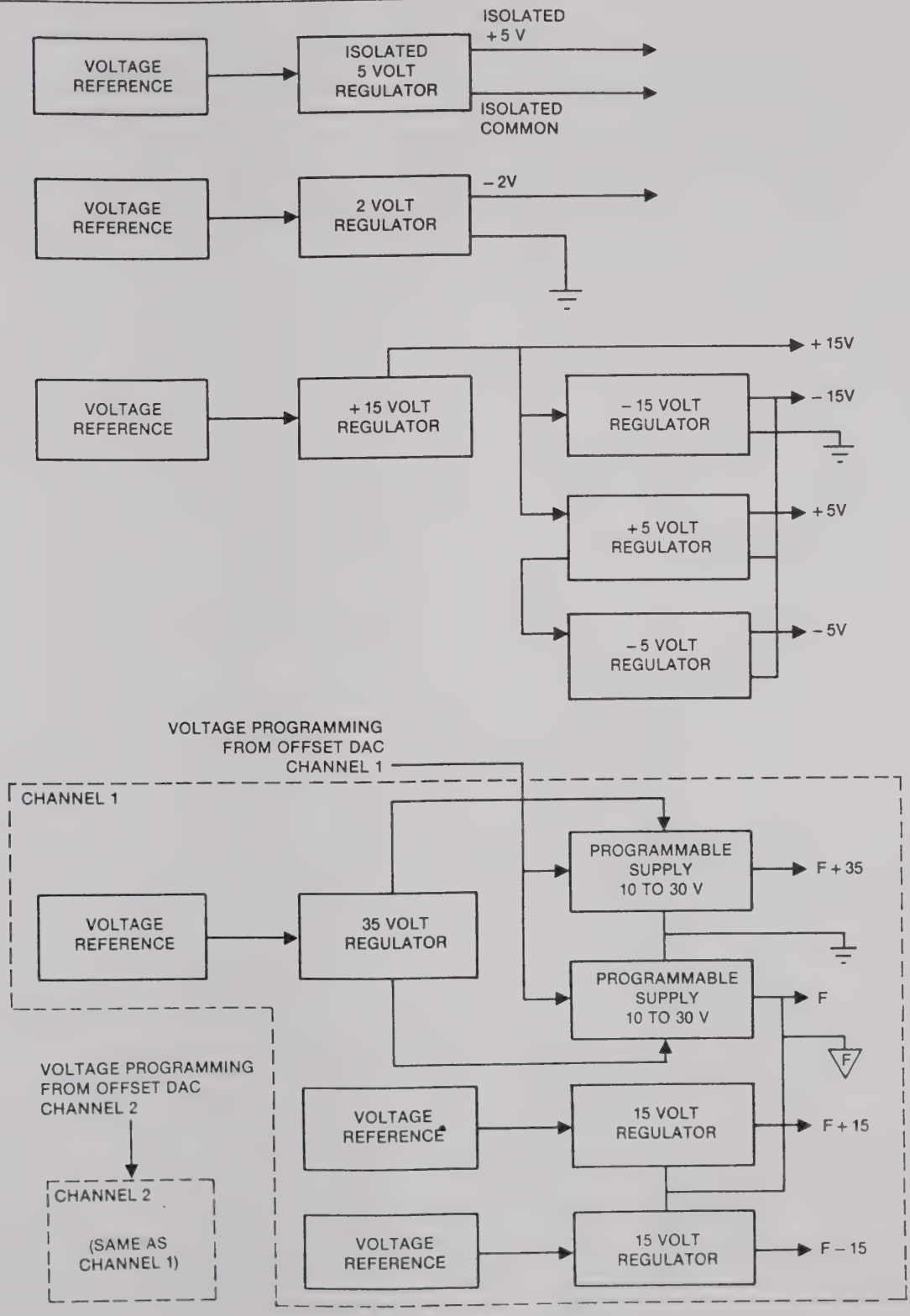


Figure 4-21. Power Supplies

3 CLOCK OUTPUT

clock output (see figure 4-3) is available as a arate output after being delayed in a Program- ble Delay Line (PDL) and buffered by a 50Ω clock lifier. The PDL is programmed by the CMOS bus nsert delays to the clock output in order to syn- onize it with the 50Ω output amplifier as various des and functions are selected.

4.14 SYNC OUTPUT

Sync output (see figure 4-3) provides a time reference establishing the beginning of the delay. The output is available as a separate output after being delayed by a PDL and buffered by a 50Ω sync amplifier. The PDL is programmed by the CMOS bus to insert delays to the sync output amplifier in order to synchronize it with the 50Ω channel output amplifier as various modes and function are selected.

SECTION 5
TROUBLESHOOTING

5.1 INTRODUCTION

Faults may be isolated to the circuit board, power supply or front panel level as shown in figure 5-1. Familiarize yourself with the 859 by reviewing the operating procedures in this manual as well as the circuit descriptions, sections 3 and 4 respectively. Successful fault isolation depends upon a thorough knowledge of the correct instrument operation.

Major groups of the various assemblies are shown in table 5-1. Fault isolation is discussed in the following paragraphs in terms of these groups. The location of boards and assemblies called out in table 5-1 are shown in figure 6-1.

Figure 5-2 is a preliminary fault isolation flow chart. By using figure 5-2 the problem may be isolated to the major group or groups within the 859 without removing the cover.

If all or part of an instrument is going to be returned to the factory for repair, include a detailed description of the specific problem. In addition, authorization from Wavetek Customer Service must be obtained in advance by calling or writing to:

Customer Service
Wavetek San Diego, Inc.
9045 Balboa Ave.
San Diego, CA 92123
Telephone (619) 279-2200
TWX: (910) 335-2007

5.2 POWER SUPPLY

If the generator is malfunctioning, power supply voltage is always the first thing to be checked. Test points for the power supply board and regulator are explained in paragraph 6.4 and 6.5. Table 5-2 shows the supply distribution to each board assembly.

If a power supply is found to be in error, it may indicate an overload or short circuit condition in the system. Consult table 5-2 for assemblies using the faulty supply. One at a time remove the boards from the instrument until the supply voltage recovers, it may be assumed the last board removed was defective and should be replaced.

5.3 MICROPROCESSOR

When microprocessor problems are suspected always check the +5V supply, refer to paragraph 5.2. If the voltage is correct use table 5-3 to troubleshoot the microprocessor board. A Hewlett-Packard 5004A Signature Analyzer may be used to verify "signature" for the microprocessor board, figure 5-3 shows the connection of the analyzer to the microprocessor board and table 5-4 describes the process while table 5-5 describes the microprocessor signatures. Replace the microprocessor board if proven defective.

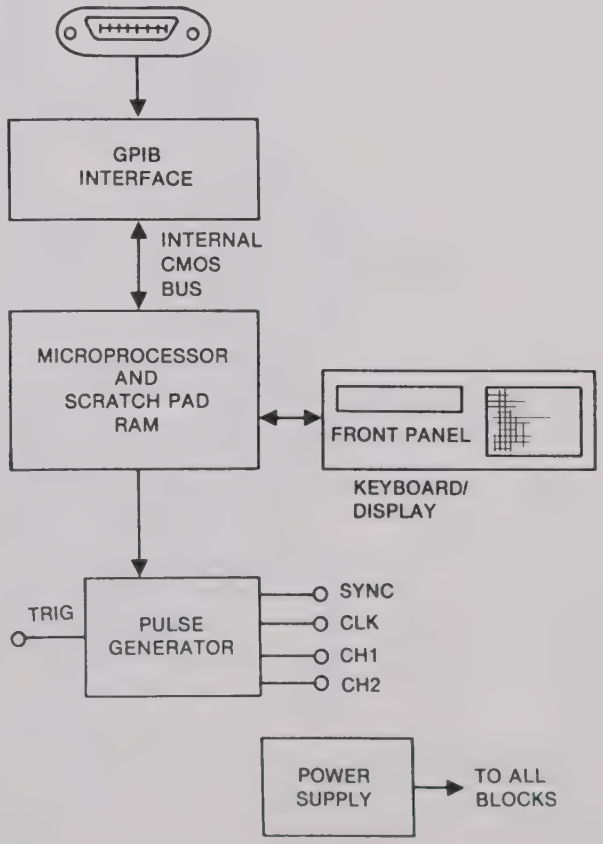


Figure 5-1. General Block Diagram

5.4 GPIB INTERFACE

Because the 859 has more than one programming channel (GPIB and front panel), it is relatively easy to isolate interface problems, refer to table 5-6. Replace the interface board if proven defective.

Table 5-1. Assembly Guide

Board Ejector Color	Assembly	Group
Red	Lo Amp (Current) Power Supply	Power Supply
None	Hi Amp (Current) Power Supply	Power Supply
White	Microprocessor	Digital
White	GPIB Interface	Digital
White	Scratch-Pad RAM	Digital
Yellow	Clock Oscillator	Pulse Generator
Green	Trigger & Burst Counter	Pulse Generator
Blue	Delay & Width	Pulse Generator
Orange	Output Amplifier	Pulse Generator
None	Display	Keyboard & Display

Table 5-3. Microprocessor Troubleshooting.

Step	Symptom	Possible Remedy
1.	859 will not power up	1. Replace RAM board 2. Replace microprocessor board 3. Replace GPIB board
2.	859 powers up and reads different GPIB address other than setting	1. Check the isolated +5V 2. Replace GPIB board 3. Replace GPIB cable
3.	859 will not talk or listen on GPIB	1. Correct the listen address setting on rear panel 2. Check the isolated +5V 3. Replace GPIB board
4.	While running, 859 resets itself and its display	1. Replace microprocessor board 2. Replace RAM board

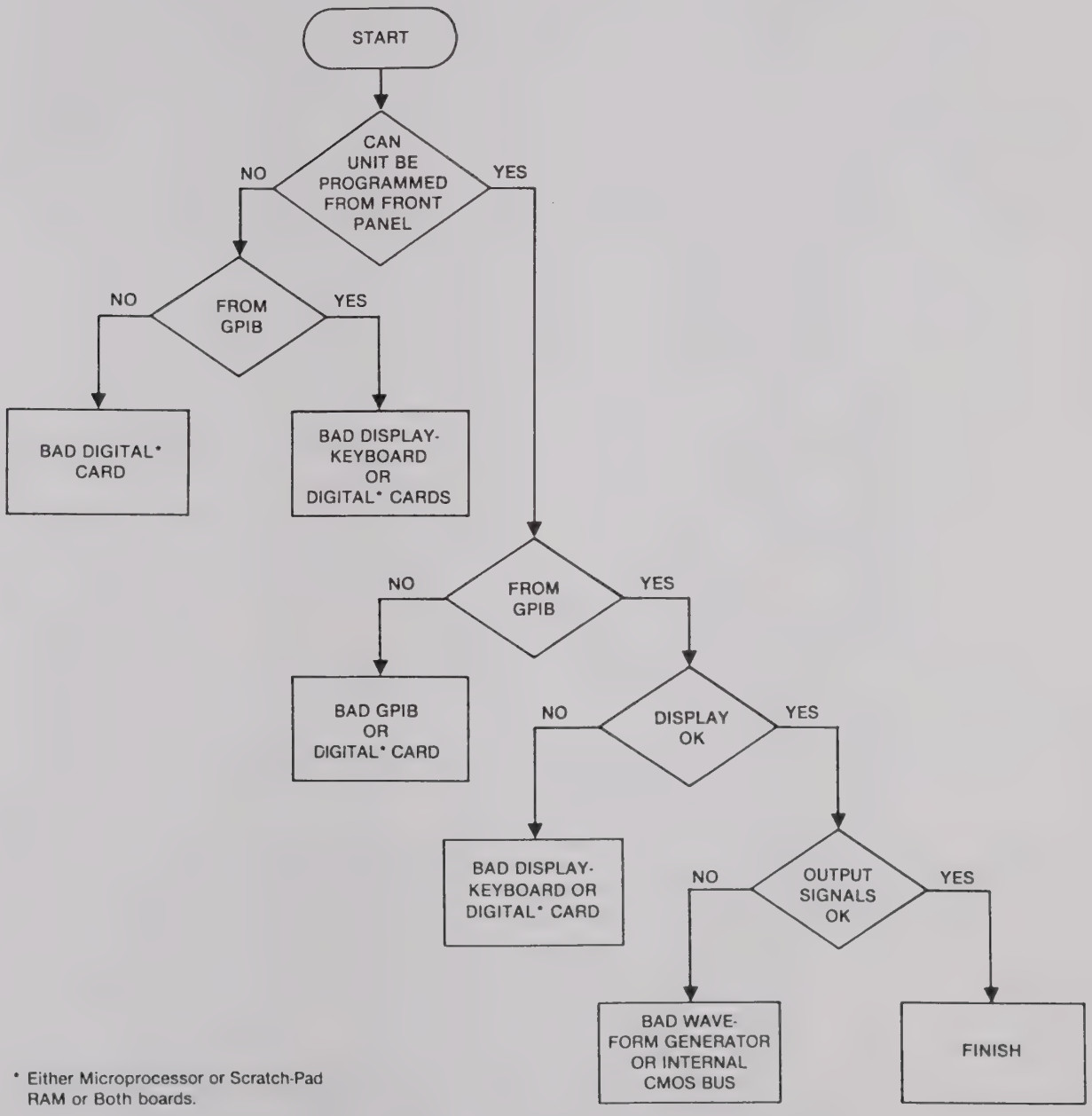


Figure 5-2. Fault Isolation Flow Chart.

			LOW CURRENT POWER SUPPLY									HIGH CURRENT POWER SUPPLY			
GROUP	ASSEMBLY	EJECTOR COLOR	ISO +5	F + 35 Ch 1	F + 35 Ch 2	F + 15 Ch 1	F − 15 Ch 1	F + 15 Ch 2	F − 15 Ch 2	+15	−15	+5	−5.2	−2	EXTENDER BOARD ASSY
POWER SUPPLY	LO AMP (CURRENT) POWER SUPPLY	RED								●	●				0517
	HI AMP (CURRENT) POWER SUPPLY	SILVER								●	●				NONE
DIGITAL	MICRO-PROCESSOR	WHITE										●			0799
	GPIB	WHITE	●									●			0799
	SCRATCH PAD	WHITE										●	●		0799
PULSE GENERATOR	CLOCK OSCILLATOR	YELLOW								●	●	●	●	●	0692
	TRIGGER & BURST	GREEN									●	●	●	●	
	DELAY & WIDTH	BLUE								●	●	●	●	●	
	OUTPUT AMPLIFIER	ORANGE		CH 1	CH 2	CH 1	CH 1	CH 2	CH 2	●	●		●	●	
FRONT PANEL	KEYBOARD & DISPLAY	N/A									●	●			NONE

Table 5-2. Power Supply Distribution

Table 5-4. Signature Analysis for the Microprocessor

Step	Description
1	Remove shunt from socket U14A.
2	Remove jumper between E20 and E21. Install at JP1 between E1 and E2.
3.	Connect analyzer as shown in figure 5-3.
4.	Power up 859.
5.	Compare signatures to those shown in table 5-5.

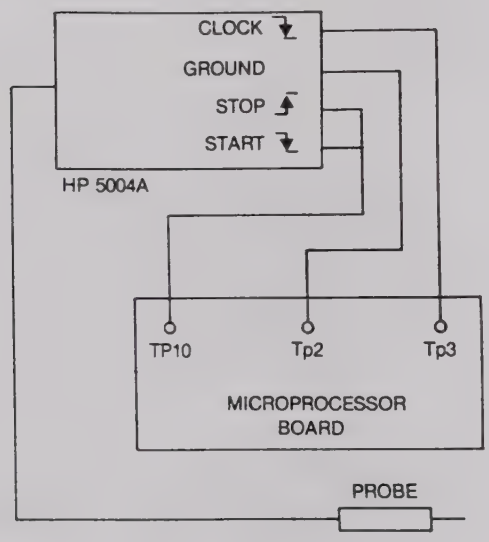


Figure 5-3. Signature Analyzer Connection

Table 5-5. Signature for the Microprocessor

Test Point	Pin Number	Signature
A0	U16A - 14	7P25
A1	U16A - 13	2A1F
A2	U16A - 12	A206
A3	U16A - 11	C133
A4	U16A - 10	8P3U
A5	U16A - 9	3319
A6	U16A - 8	7C47
A7	U16A - 7	C25F
A8	U16A - 6	5H21
A9	U16A - 5	19H6
A10	U16A - 4	HP66
A11	U16A - 3	7A70
A12	U16A - 2	——
A0	U16B - 19	UF4C
A1	U16B - 18	A872
A2	U16B - 17	2068
A3	U16B - 16	335H
A4	U16B - 15	0F51
A5	U16B - 14	C177
A6	U16B - 13	U929
A7	U16B - 12	3032
A8	U15 - 19	H64U
A9	U15 - 18	9CC8
A10	U15 - 17	5F08
A11	U15 - 16	U81P
A12	U15 - 15	826P
0_1	U14A - 9	U213
0_2	U14A - 10	9C81
0_3	U14A - 11	U7F5
0_4	U14A - 12	4UT0
0_5	U14A - 13	PP76
0_6	U14A - 14	P530
0_7	U14A - 15	6063
0_8	U14A - 16	H8H6

NOTE: These signatures are valid for wake-up or reset mode only.

Table 5-6. GPIB Troubleshooting

Symptom	Discussion
1. When addressed as a listener or talker, tne 859 does not display LSN or TLK annunciator.	Find the GPIB listen and talk addresses by pushing the ADRS key. They will be displayed. Program the controller to send the listen address. (The HP9825 controller message is wrt 7xx, where xx is the 859 address.) LSN or LSN and REM annunicator should appear on the display; if not, the malfunction is in the GPIB interface board. The talk address problem is similarly dealt with.
2. Displayed parameters values differ from GPIB programmed values.	Use the CMD RCL key to display the programming received by the post-interface circuits. If this differs from GPIB programmed values, duplicate the programming by using the front panel controls. Correct display isolates the malfunction to the GPIB interface board.

5.5 FRONT PANEL

The front panel assembly contains circuitry for two distinct functions; display and keyboard, both communicating with the microprocessor through the data and address bus. Because of the intimate relationship of the front panel and microprocessor, it can be difficult to isolate a problem to the area. Refer to table 5-7 for troubleshooting information.

5.6 SCRATCH PAD RAM

When a RAM problem is suspected the following troubleshooting procedure is used to verify the problem.

First verify that proper supply voltages are present at the RAM board, refer to table 5-2 for power supply distribution. If all voltages are present use table 5-3 to troubleshoot the RAM board.

A Hewlett-Packard 5004A Signature Analyzer may be used to verify the "signature" of the RAM board. Table 5-8 explains the analyzer connection while table 5-9 describes the RAM signatures.

Replace the RAM board if proven defective.

5.7 INTERNAL CMOS BUS

All of the internal programming to the pulse generator is supplied through the 16 internal bus lines. It takes only one defective receiver-driver to hang-up an entire line. A defective receiver-driver can cause incorrect generator response.

A defective receiver-driver can be located by removing and replacing one board at a time; the bus voltage will return to normal when the defective board is removed.

Tables 5-10, 5-11 and 5-12 give information relative to the operation of the internal CMOS bus. Data and address are presented to the appropriate boards in a predetermined sequency. Table 5-11 describes the data sending sequence and the appropriate address and data; the data sending sequence is initiated by an execute command. While actual bus location is described in table 5-10. Each data byte (control bit code) is described in table 5-12.

5.8 PULSE GENERATOR

If the pulse generator is malfunctioning, first check the power supply voltages (refer to paragraph 5.2) Second, some problems are due to the system being out of calibration, therefore an attempt should be made to calibrate the generator prior to troubleshooting (refer to section 6).

Table 5-13 describes a series of symptoms and possible cures for pulse generator problems.

Table 5-7. Front Panel Troubleshooting

Symptom	Discussion
1. When power is first turned on, the front panel readout displays "SELF TEST". After a short delay, the microprocessor commands the front panel to display "WAVETEK 859". The message is not displayed.	If this message never appears, the problem can be on any of the digital boards. Most likely it is not a front panel problem. While a front panel failure could cause the front panel not to accept data, it is much more likely the microprocessor never reached the portion of the operating program that causes the initial display. Replace the Microprocessor, GPIB and Scratch Pad (RAM) board one at a time. Test the 859 with each replacement.
2. After the turn-on delay, the initial random characters are replaced by another meaningless display.	The microprocessor is reaching the front panel. Examine this message carefully for clues as to the possible problem; for example, "V@VDTDJ 848" instead of "WAVETEK 859" would indicated the "1" bit of the data word was hung in a false condition. This could be occurring in the front panel bus receivers, memory or in the display component itself. Another type of failure mode might be "WAWATETE 8585" indicating a hung "2" bit on the address lines driving the memory IC. In any case, the malfunction is most likely in the front panel.
3. The display is missing segments of characters.	The problem is most likely the display component, or the RAM chips. Replace the front panel.
4. The keyboard "beeps" normally when a key is depressed, but the processor ignores it (no response on the display).	The problem may be in the front panel or in the microprocessor. command the 859 via the GPIB and check for proper operaton. If the 859 cannot be commanded by any means, the problem is most likely not in the front panel. A front panel address or data bus driver or receiver could fail in a manner to permanently hang a bus line, preventing the microprocessor from operating properly. Unplug the front panel from the mother board J18 with power off. Turn power back on and again try to command the 859 via GPIB. If the 859 runs properly, the problem is in the front panel.
5. The keyboard fails to "beep", but commands the 859 properly.	The problem is in the circuitry associated with the audio sounder. Replace the front panel.
6. The keyboard neither beeps or commands the 859 but 859 works properly with the GPIB interface.	The problem is with the keyboard encoder, or the keyboard membrane switch itself. Replace the front panel.

Table 5-8. Signature Analysis For Scratch Pad RAM

Step	Description
1.	Connect Analyzer as shown in Figure 5-4.
2.	Power up the 859.
3.	On RAM board short TP1 to ground
4.	Compare signatures to those shown in Table 5-9.

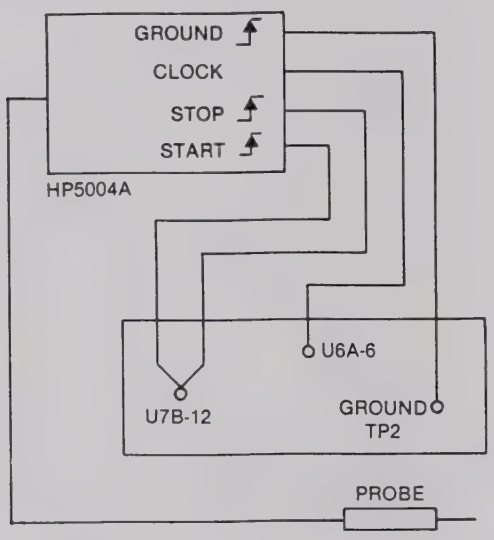


Figure 5-4. Signature Analyzer Connection

Table 5-9. Scratch Pad RAM Signature

Test Point	Pin Number	Signature
+5V		6PCP
DO 0	U11B-5	4980
DO 1	U11B-7	A612
DO 2	U11B-9	9964
DO 3	U11B-11	A7PC
DO 4	U12B-5	3POP
DO 5	U12B-7	2A63
DO 6	U12B-9	P9F6
DO 7	U12B-11	430U
CA 0	U9B-5	2595
CA 1	U9B-7	1F8F
CA 2	U9B-9	U97F
CA 3	U9B-11	5A34
CA 4	U10B-5	91FC
CA 5	U10B-7	3CPF

NOTE: These signatures are valid for power-on or wake-up mode only.

Table 5-10. Internal CMOS Bus Location

Description	Bus Line	Connector Pin Numbers *
Strobe	STRB 1	4B
	STRB 2	3A
Address Line	AA5	2B
	AA4	3B
	AA3	5B
	AA2	6B
	AA1	7B
	AA0	8B
Data Line	AD7	10B
	AD6	11B
	AD5	12B
	AD4	13B
	AD3	14B
	AD2	15B
	AD1	16B
	AD0	17B

* Pin numbers refer to connectors J4 through J9, located on the mother board.

Table 5-11. Internal Bus Data Allocation

DATA SENDING SEQUENCE	ADDRESS						DATA								CHANNEL
	AA5	AA4	AA3	AA2	AA1	AA0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
0	0	0	0	0	0	0									Both
1	0	0	0	0	0	1									
2	0	0	0	0	1	0	BU15	BU14	BU13	BU12	BU11	BU10	BU9	BU8	
							Burst Digit 3#				Burst Digit 2#				
3	0	0	0	0	1	1	BU7	BU6	BU5	BU4	BU3	BU2	BU1	BU0	
							Burst Digit 1#				Burst Digit 0*				
4	0	0	0	1	0	0		A6	A5	A4	A3	A2	A1	A0	
								Mode				Trig Format			
5	0	0	0	1	0	1	**			B4	B3	B2	B1	B0	
										Mode					
6	0	0	0	1	1	0						PDS2	PDS1	PDS0	
												Mode			
7	0	0	0	1	1	1									
8	0	0	1	0	0	0	FR7	FR6	FR5	FR4	FR3	FR2	FR1		
							Frequency DAC B6-B0								
9	0	0	1	0	0	1			S3	S2	S1	S0	FR9	FR8	
									Prescaler				Freq DAC		
10	0	0	1	0	1	0		OR6	OR5	OR4	OR3	OR2	OR1	OR0	
								Frequency Range							
11-15	0	0	1	X	X	X									CH1 ONLY
16	0	1	0	0	0	0	WI11	WI10	WI9	WI8	DE11	DE10	DE9	DE8	
							Width Control MSD				Delay Control MSD				
17	0	1	0	0	0	1	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	
							Delay Control Digit 2				Delay Control Digit 1				
18	0	1	0	0	1	0	WI7	WI6	WI5	WI4	WI3	WI2	WI1	WI0	
							Width Control Digit 2				Width Control Digit 1				
19	0	1	0	0	1	1	WIR5	WIR4	DER5	DER4	DER3	DER2	DER1	DER0	
							Width Range		Delay Range						
20	0	1	0	1	0	0	C3	C2	C1	C0	WIR3	WIR2	WIR1	WIR0	
							Function				Width Range				
21	0	1	0	1	0	1			PDW4	PDD4	PDD3	PDD2	PDD1	PDD0	
									WDL	Delay Delay Line					
22	0	1	0	1	1	0					PDW3	PDW2	PDW1	PDW0	
											Width Delay Line				
23	0	1	0	1	1	1									
24	0	1	1	0	0	0		Int Use ***	AF3	AF2	TR0	AT3	AT2	AT1	
									On/Off	50Ω	Norm/ Comp	Amplitude Range			

Table 5-11. Internal Bus Data Allocation (Continued)

DATA SENDING SEQUENCE	ADDRESS						DATA								CHANNEL
	AA5	AA4	AA3	AA2	AA1	AA0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
25	0	1	1	0	0	1	NOS	AF0			OS9	OS8	AMP9	AMP8	CH1 ONLY
							Ofst Pol	‡			Offset		Amplitude		
26	0	1	1	0	1	0	OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0	
							Offset DAC								
27	0	1	1	0	1	1	AMP7	AMP6	AMP5	AMP4	AMP3	AMP2	AMP1	AMP0	
							Amplitude DAC								
28	0	1	1	1	0	0	TE11	TE10	TE9	TE8	LE11	LE10	LE9	LE8	
							Trailing Edge DAC				Leading Edge DAC				
29	0	1	1	1	0	1	TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0	
							Trailing Edge DAC								
30	0	1	1	1	1	0	LE7	LE6	LE5	LE4	LE3	LE2	LE1	LE0	
							Leading Edge DAC								
31	0	1	1	1	1	1			TR5	TR4	TR3	TR2	TR1	TR0	
									Transition Range						
32	1	0	0	0	0	0									CH 2 ONLY
47	1	0	1	1	1	1									
48	1	1	0	0	0	0	WI11	WI10	WI9	WI8	DE11	DE10	DE9	DE8	
							Width Control MSD				Delay Control MSD				
49	1	1	0	0	0	1	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	
							Width Control Digit 2				Width Control Digit 1				
50	1	1	0	0	1	0	WI7	WI6	WI5	WI4	WI3	WI2	WI1	WI0	
							Width Control Digit 2				Width Control Digit 1				
51	1	1	0	0	1	1	WIR5	WIR4	DER5	DER4	DER3	DER2	DER1	DER0	
							Width Range		Delay Range						
52	1	1	0	1	0	0	C3	C2	C1	C0	WIR3	WIR2	WIR1	WIR0	
							Function				Width Range				
53	1	1	0	1	0	1			PDW4	PDD4	PDD3	PDD2	PDD1	PDD0	
									WDL‡‡		Delay Delay Line				
54	1	1	0	1	0	1					PDW3	PDW2	PDW1	PDW0	
											Width Delay Line				
55	1	1	0	1	1	0									
56	1	1	1	0	0	0		Int Use	AF3 On/Off	AF2 50Ω	TR0	AT3	AT2	AT1	
											Norm/ Comp	Amplitude Range			
57	1	1	1	0	0	1	NOS	AF0					AMP9	AMP8	
							Ofst Pol				Offset		Amplitude		
58	1	1	1	0	1	0	OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0	
							Offset DAC								
59	1	1	1	0	1	1	AMP7	AMP6	AMP5	AMP4	AMP3	AMP2	AMP1	AMP0	
							Amplitude DAC								

Table 5-11. Internal Bus Data Allocation (Continued)

DATA SENDING SEQUENCE	ADDRESS						DATA								CHANNEL
	AA5	AA4	AA3	AA2	AA1	AA0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	
							TE11	TE10	TE9	TE8	LE11	LE10	LE9	LE8	CH2 ONLY
60	1	1	1	1	0	0	Trailing Edge DAC				Leading Edge DAC				
							TE7	TE6	AMP6	TE4	TE3	TE2	TE1	TE0	
61	1	1	1	1	0	1	Trailing Edge DAC								
							LE7	LE6	LE5	LE4	LE3	LE2	LE1	LE0	
62	1	1	1	1	1	0	Leading Edge DAC								
									TR5	TR4	TR3	TR2	TR1	TR0	
63	1	1	1	1	1	1			Transition Range						

* Burst digits are computed by 10,000 − burst count.

** Software Bit: 1 if Trig, Burst, or Time Interval Mode is selected.

*** Used by Software to determine if 50Ω backmatch should be disconnected when the output is turned on.

‡ If Amplitude is < 5V and upper level is > 5V then AFO is set to 1 and offset is increased 100 × attenuation.

Example: If output amplitude is between 1V and 2V then ÷ 5 attenuation will be selected and offset will be increased by 20; i.e., 100 × 1/5.

‡‡ Width delay line.

Table 5-12. Control Bit Code Definition

A. MODE (Address 4, 5, 6)

Mode	AG	A5	A4	A3	B4	B3	B2	B1	B0	PDS2	PDS1	PDS0
Cont	1	1	1	0	1	1	1	1	0	1	1	0
Trig	1	1	0	1	0	1	1	0	1	0	1	0
Gate	1	1	1	0	0	1	0	0	1	1	1	1
Burst	1	1	1	0	0	0	0	0	1	1	1	1
EW	1	0	1	1	0	1	1	0	1	0	0	0
TI	0	1	1	1	0	0	0	0	1	0	0	1

B. FUNCTION (Address 20, 52)

Function	C3	C2	C1	C0
Single	0	1	1	0
Double	0	1	0	0
Square	0	0	1	1
Inhibit	1	1	1	1

C. TRIGGER FORMAT (Address 4)

Format	A2	A1	A0
+ Slope	1	0	1
– Slope	0	1	1
Man	1	1	0

D. FREQUENCY PRESCALER (Address 9)

Program Value	Range	÷ N	S3	S2	S1	S0
25-50	MHz	÷ 1	1	0	0	0
12.5 – 24.9	Any	÷ 2	0	1	0	1
10 – 12.4	Any	÷ 4	0	0	1	1
5 – 9.99	Any	÷ 5	0	0	1	0
2.5 – 4.49	Any	÷ 10	0	0	0	1

E. FREQUENCY RANGE (Address 10)

-10^N	OR6	OR5	OR4	OR3	OR2	OR1	OR0
N = 0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	0
2	1	1	1	1	1	0	0
3	1	1	1	1	0	0	0
4	1	1	1	0	0	0	0
5	1	1	0	0	0	0	0
6	1	0	0	0	0	0	0
7	0	0	0	0	0	0	0

F. FREQUENCY DAC (Address 8, 9)

FREQ	FR9	FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1	COUNT
25.0 MHz	0	0	0	0	0	0	0	0	0	0
50.0 MHz	1	1	1	1	1	0	1	0	0	500

Table 5-12. Control Bit Code Definition (Continued)

G. OFFSET POLARITY (Address 25, 57)

Polarity	Nos
+	1
0	0
–	0

H. OFFSET DAC (Address 25, 26, 57, 58)

	OS9	OS8	OS7	OS6	OS5	OS4	OS3	OS2	OS1	OS0	AF2
0.0V ↓	0	0	0	0	0	0	0	0	0	0	0 ↓
10.0V	1	1	1	1	1	0	1	0	0	0	0
0.0V ↓	0	0	0	0	0	0	0	0	0	0	1 ↓
20.0V	1	1	1	1	1	0	1	0	0	0	1

I. AMPLITUDE DAC (Address 26, 27, 58, 59)

	AMP 9	AMP 8	AMP7	AMP6	AMP 5	AMP4	AMP 3	AMP 2	AMP 1	AMP 0	DECIMAL VALUE
Top of Range ↓	1	1	1	1	1	0	1	0	0	0	1000
Bottom of 2:1 Range ↓	0	1	1	1	1	1	0	1	0	0	500
Bottom of 2.5:1 Range	0	1	1	0	0	1	0	0	0	0	400

J. AMPLITUDE RANGE (ATTENUATION) (Address 24, 56)

		×10	×5	×2	INT 50Ω
Amplitude	Attenuation	AT3	AT2	AT1	AF2
10V – 20V	1	0	1	0	1
5V – 10V	1	0	1	0	0
2V – 5V	.5	0	1	1	0
1V – 2V	.2	0	0	0	0
.4V – 1V	0	0	1	0	0
.2V – .4V	.05	1	1	1	0
.1V – .2V	.02	1	0	0	0
.04V – .1V	.01	1	0	1	0
		High True Logic	Low True Logic	High True Logic	Low True Logic

Table 5-12. Control Bit Code Definition (Continued)

J. TRANSITION RANGE (Address 31, 63)

RANGE	TR5	TR4	TR3	TR2	TR1	TR0
4 ns - 100 ns	1	1	1	1	1	1
50 ns - 2.5 μs	0	1	1	1	1	0
500 ns - 25 μs	0	1	1	1	0	1
5 μs - 250 μs	0	1	1	0	1	1
50 μs - 2.5 ms	0	1	0	1	1	1
500 μs - 25 ms	0	0	1	1	1	1

K. LEADING/TRAILING EDGE DACS * (Address 24, 29, 30, 60, 61, 62)

PROGRAM VALUE	RATIO	TE11	TE10	TE9	TE8	TE7	TE6	TE5	TE4	TE3	TE2	TE1	TE0	Decimal Value
5.00	1	1	1	1	1	1	1	1	1	1	1	1	1	4095
10.0	2	1	0	0	0	0	0	0	0	0	0	0	0	2048
50.0	10	0	0	0	1	1	0	0	1	1	0	1	0	410
100	20	0	0	0	0	1	1	0	0	1	1	0	1	205
250	50	0	0	0	0	0	1	0	1	0	0	1	0	82

* *NOTE: When complement is true, data for the leading and trailing edges are interchanged by the microprocessor.*

L. DELAY RANGE (Address 19, 51)

RANGE	DER5	DER4	DER3	DER2	DER1	DER0
0 - 34 ns	1	1	1	1	1	1
35 - <20 μs	1	1	1	1	1	0
20 μs - <100 μs	1	1	1	1	0	0
100 μs - <1 ms	1	1	1	0	0	0
1 ms - <10 ms	1	1	0	0	0	0
10 ms - <100ms	1	0	0	0	0	0
100 ms - <1s	0	0	0	0	0	0

M. DELAY DELAY LINE (Address 21, 53)

RANGE	PDD4	PDD3	PDD2	PDD1	PDD0
0 - 24 ns	a	a	a	a	a
25 ns - 20 μs	b	b	b	b	b
All others	0	0	0	0	0
	16 ns	8 ns	4 ns	2 ns	1 ns

NOTES: a. The values assigned for PDD0 through PDD4 are the binary equivalent of a decimal number which is equal to the programmed delay and SWI (located on scratch pad RAM board). PDD0 is the LSB.

b. The values assigned for PDD0 through PDD4 are the binary equivalent of the decimal number equal to:

$$20 \times \text{FRACTIONAL PART OF } \left[\frac{\text{Delay} + SW1 + SW2 - 26\ ns}{20\ ns} \right]$$

Values for Delay, SW1, and SW2 are in ns.

Table 5-12. Control Bit Code Definition (Continued)

N. DELAY COUNTER (Address 16, 17, 48, 49)

RANGE	MSD				DIGIT 2				LSD				DECIMAL
	DE11	DE10	DE9	DE8	DE7	DE6	DE5	DE4	DE3	DE2	DE1	DE0	VALUE
20 μs - 100 μs	0	0	1	0	0	0	0	0	0	0	0	0	200
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
100 μs - 1 ns	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
1 ms - 10 ms	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
10 ms - 100 ms	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
100 ms - 1S	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999

NOTE: The value sent to the delay counter is a binary number representation of the integer value of $D_N = [Delay + SW- + SW2 - 26]/20$ *where SW1 + SW2 and Delay are in ns. For channel 2, SW5 and SW6 should be substituted for SW1 and SW2 respectively.*

O. WIDTH DELAY LINE (Address 22, 54)

RANGE	PDW4	PDW3	PDW2	PDW1	PDW0
0 - 34 ns	a	a	a	a	a
35 ns - 20 μs	b	b	b	b	b
All others	0	0	0	0	0

NOTES:

a. The values assigned for PDD0 through PDW4 are the binary equivalent of the following number:

$N_{WDL} = W^*_{Hardware} + SW_3 - 13\ ns$

All values are in ns and SW_3 *is located on the scratch pad RAM board.*

b. The values assigned for PDD0 through PDW4 is the binary equivalent of the following number:

$N_{WDL} = 20 \times$ *FRACTIONAL PART OF:*

$$\left[\frac{W^*_{Hardware} + SW_3 + SW_4 - 41\ ns}{20\ ns} \right]$$

$W_{HARDWARE}$, $SW_3 + SW_4$ *are in ns.*

$^* W_{Hardware} = Width_{Programmed} + 0.625\ [Lead\ Edge_{Prog} - Trail\ Edge_{Prog}]$

Table 5-12. Control Bit Code Definition (Continued)

P. WIDTH COUNTER (Address 16, 18, 48,50)

RANGE	MSD				DIGIT 2				LSD				DECIMAL
	WI11	WI10	WI9	WI8	WI7	WI6	WI5	WI4	WI3	WI2	WI1	WI0	VALUE
20 μs - 100 μs	0	0	1	0	0	0	0	0	0	0	0	0	200
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
100 μs - 1 ms	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
1 ms - 10 ms	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
10 ms - 100 ms	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999
100 ms - 1s	0	0	0	1	0	0	0	0	0	0	0	0	100
↓	1	0	0	1	1	0	0	1	1	0	0	1	999

NOTES:a .The value sent to the width counter is:

$$W_N = \text{INTEGER PART OF:}$$

$$\left[\frac{W_{Hardware} + SW_3 + SW_4 - 41\ ns}{20\ ns} \right]$$

For channel 2, SW_7 and SW_8 should be substituted for $SW_3 + SW_4$ respectively.

* $W_{Hardware} = Width_{Programmed} + 0.625\ [Lead\ Edge_{Prog} - Trail\ Edge_{Prog}]$

Q. WIDTH RANGE (Address 19, 20, 51, 52)

RANGE	WIR5	WIR4	WIR3	WIR2	WIR1	WIR0
0 - 34 ns	1	1	1	1	1	1
35 ns - 20 μs	1	1	1	1	1	0
20 μs - 100 μs	1	1	1	1	0	0
100 μs - 1 ms	1	1	1	0	0	0
1 ms - 10 ms	1	1	0	0	0	0
10 ms - 100 ms	1	0	0	0	0	0
100 ms - 1s	0	0	0	0	0	0

Table 5-12. Control Bit Code Definition (Continued)

R. BURST LENGTH (Address 2, 3)

	DIGIT 4				DIGIT 3				DIGIT 2				DIGIT 1			
BURST COUNT	BU 15	BU 14	BU 13	BU 12	BU 11	BU 10	BU 9	BU 8	BU 7	BU 6	BU 5	BU 4	BU 3	BU 2	BU 1	BU 0
0001 ↓	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1
0009 ↓	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	1
0010 ↓	1	0	0	1	1	0	0	1	1	0	0	1	0	0	0	0
0090 ↓	1	0	0	1	1	0	0	1	0	0	0	1	0	0	0	0
0100 ↓	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
0090 ↓	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
1000 ↓	1	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
9000 ↓	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
9999 ↓	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	1
10,000	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Digit Value = 10,000 – Programmed Burst Count

Table 5-13. Pulse Generator Troubleshooting

Symptom	Discussion	Probable Cause	Remedy
Frequency failure: No output at some frequencies. Frequency not monotonic. Inaccurate frequencies.	Check output in ⊓ continuous mode to bypass problems caused by the delay-width board. Test programming bits using Tables 5-11 and 5-12.	Defective clock board. Defective internal CMOS bus. Defective microprocessor board.	Replace defective clock board or microprocessor board.
Delay problems, single or double pulse functions.	Check delay-width board or internal CMOS bus. Check A4 on burst board is detective. Exchange boards from second channel, if available, to isolate defective.	Defective delay-width board. Defective internal CMOS bus. Defective microprocessor board.	Swap or replace delay-width board or microprocessor board.
Width problems, single or double pulse functions.	Check in ⊓ function with 4 ns leading and trailing edge transitions. Exchange boards from second channel, if available, to isolate defective board	Defective delay-width board. Defective internal CMOS bus. Defective microprocessor board.	Swap or replace output amplifier or microprocessor board.
Transition time problems, leading edge or trailing edge.	Check in continuous ⊓ function. Exchange boards from second channel, if available, to isolate defective board.	Defective output amplifier board. Defective internal CMOS bus. Defective microprocessor board.	Swap or replace output amplifier or microprocessor board.
Output level problem, upper and lower level.	Terminate output into precision 50Ω. Check level with 4 ns transition time in continuous ⊓ mode.	Defective output amplifier board. Defective internal CMOS bus. Defective microprocessor board.	Swap or replace output amplifier or microprocessor board.
No output in any mode or function.	Usually output amplifier failure. If upper level can be varied, it may indicate a loss of drive signal to the output amplifier. Loss of drive signal may be caused by defective delay-width or burst boards.	Defective output amplifier. Disconnected output connector. Defective delay-width board. Defective burst board. Defective internal CMOS bus.	Swap or replace output amplifier board, delay-width board, burst board, microprocessor board or check power supply.
Burst mode inoperative or incorrect count.	Check burst in ⊓ function, with leading edge and trailing edge at 4 ns.	Defective burst card. Defective internal CMOS bus. Defective microprocessor board. Defective clock board.	Replace burst board. Replace microprocessor board. Replace clock board.
Time interval mode inoperative or incorrect.	Check time interval with leading edge and trailing edge at 4 ns.	Defective burst board. Defective clock board. Defective microprocessor board. Defective internal CMOS bus.	Replace burst board. Replace microprocessor board.

Table 5-13. Pulse Generator Troubleshooting (Continued)

Symptom	Discussion	Probable Cause	Remedy
Mode or modes inoperative.	Exchange burst board which contains most of the mode logic. Depending on the particular mode, almost any board may be involved.	Defective burst board. Defective microprocessor board. Defective internal CMOS bus.	Replace delay-width board. Replace microprocessor board.
Function or functions inoperative.	Exchange delay-width board from second channel, if available, to isolate defective board.	Defective delay-width board. Defective microprocessor board. Defective internal CMOS bus.	Replace burst board. Replace microprocessor board.
Trigger input inoperative.	Check trigger level control (should be centered). Check coax connections to burst board are connected properly.	Defective burst board. Defective microprocessor. Defective internal CMOS bus.	Replace burst board. Replace microprocessor board.
Trigger format inoperative.	Check input trigger level (within specifications). Note: ⊣⊔ and ⊔⊢ reverse phase between trigger input and output; not between sync and output.	Defective burst board. Defective microprocessor board. Defective internal CMOS bus.	Swap or replace output amplifier board. Replace microprocessor board.
Normal/complement output inoperative.	Exchange outplut amplifier board with second channel, if availabe, to isolate defective board.	Defective output amplifier board. Defective microprocessor board. Defective internal CMOS bus.	Swap or replace output amplifier board. Replace microprocessor.
Output on/off inoperative.	Exchange output amplifier board with second channel, if available to isolate defective board.	Defective output amplifier board. Defective microprocessor board. Defective internal CMOS bus.	Replace burst board. Replace microprocessor board.
Sync output inoperative.	Check sync output connector from board for a firm connection.	Defective burst board. Defective microprocessor board. Defective internal CMOS bus.	Replace burst board. Replace clock board. Replace microprocessor board.
Clock output inoperative.	Check clock output connector from burst board for a firm connection.	Defective burst board. Defective microprocessor board. Defective internal CMOS bus.	Replace burst board. Replace microprocessor board.

REAR PANEL BNC LEGEND	
CONNECTOR	DESTINATION
J27, TRIG IN	A4-J4, BURST BD
J26, SYNC OUT	A4-J3, BURST BD
s25, CLOCK OUT	A4-J2, BURST BD
J23, CH 1 OUTPUT	A9-J1, CH 2 OUTPUT AMPL
J24, CH 2 OUTPUT (OPTIONAL)	A16-J1, CH2 OUTPUT AMPL (OPTIONAL)

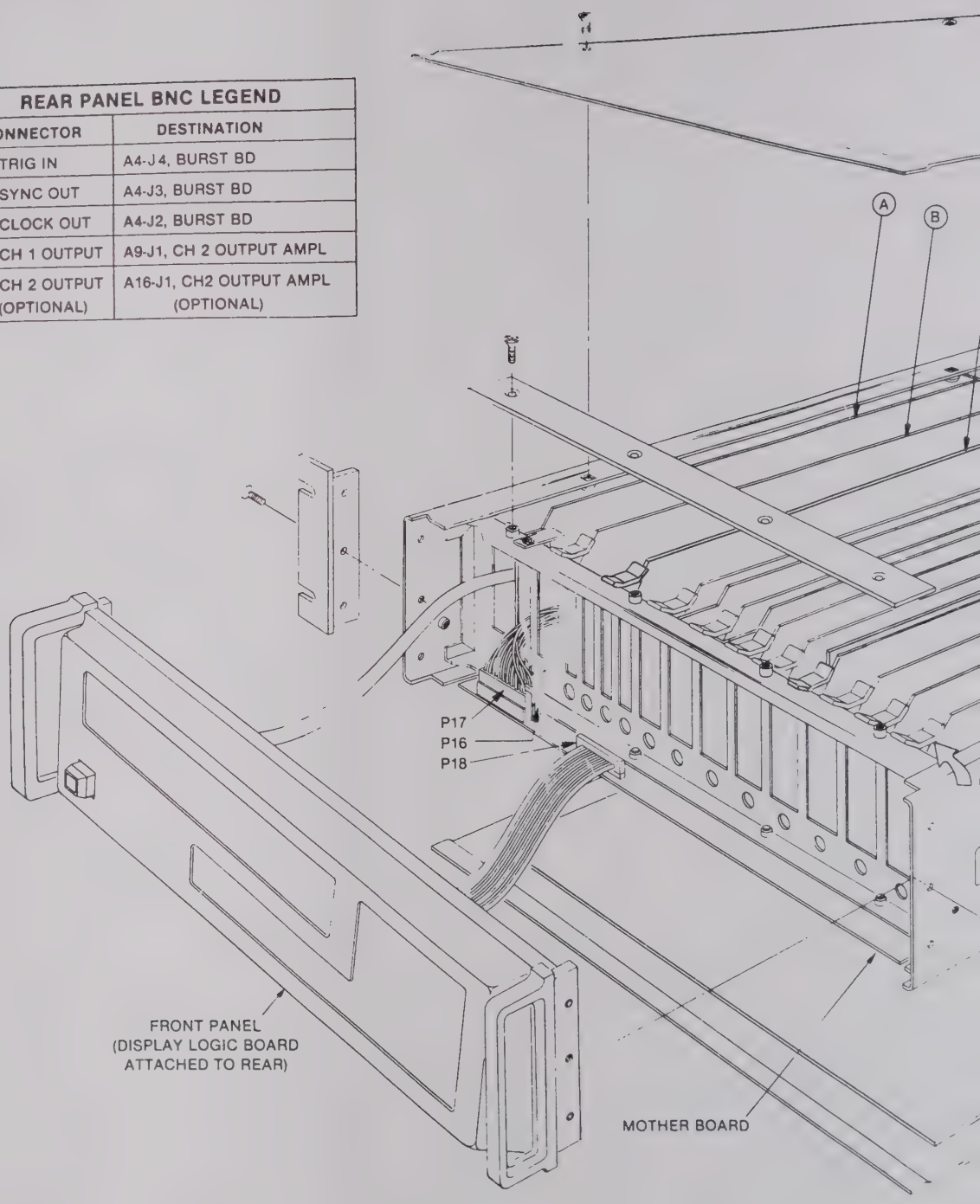
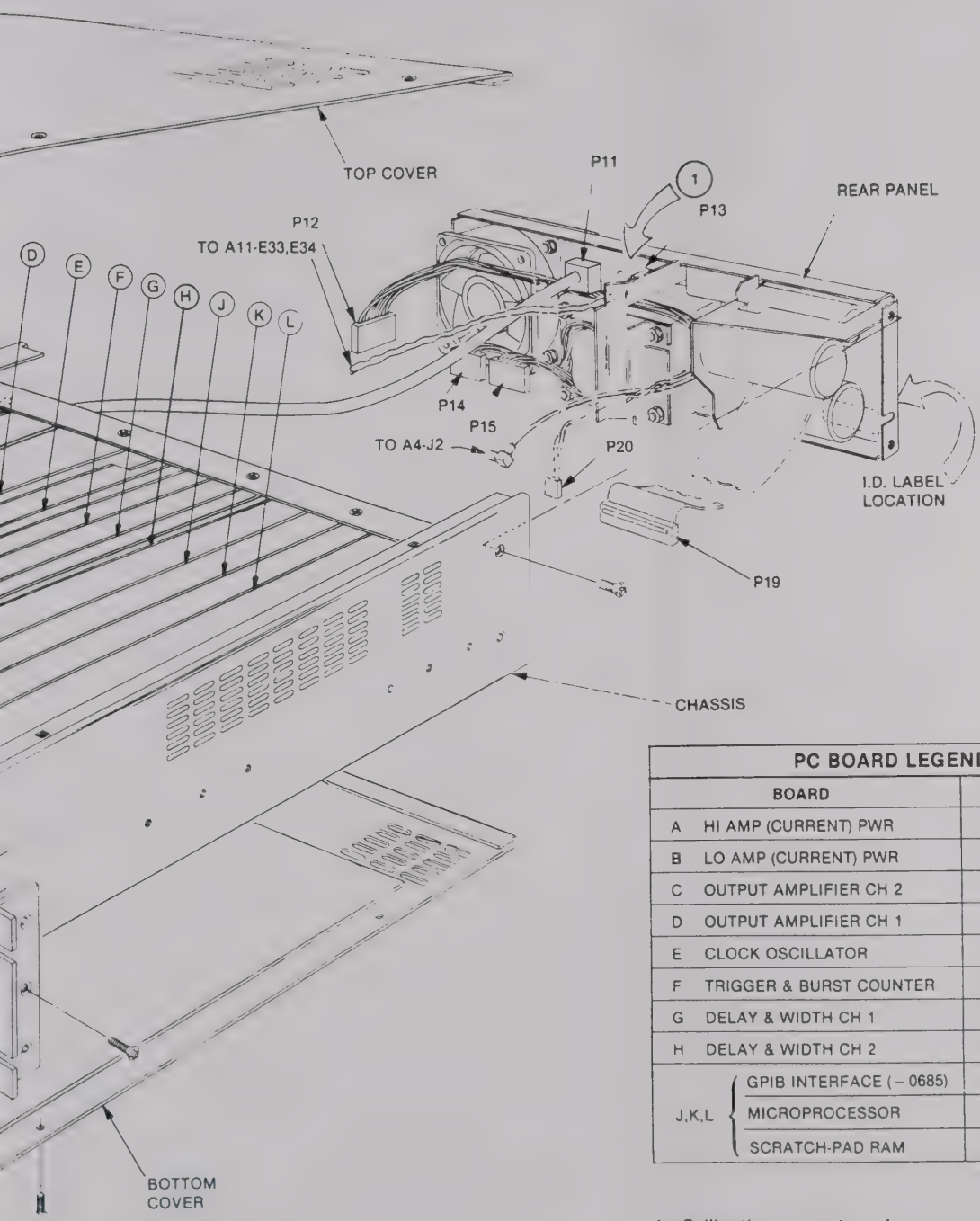
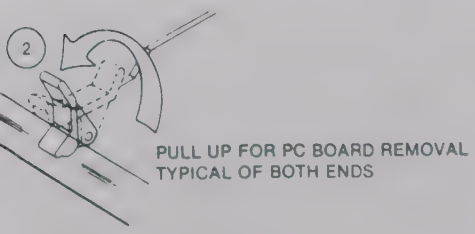


Figure 6-1. Circuit Board and Connector Locations





PC BOARD LEGEND		
BOARD		EJECTOR COLOR
A	HI AMP (CURRENT) PWR	NONE
B	LO AMP (CURRENT) PWR	RED
C	OUTPUT AMPLIFIER CH 2	ORANGE 1
D	OUTPUT AMPLIFIER CH 1	ORANGE 1
E	CLOCK OSCILLATOR	YELLOW
F	TRIGGER & BURST COUNTER	GREEN
G	DELAY & WIDTH CH 1	BLUE 1
H	DELAY & WIDTH CH 2	BLUE 2
J,K,L	GPIB INTERFACE (– 0685)	WHITE 3
J,K,L	MICROPROCESSOR	WHITE 3
J,K,L	SCRATCH-PAD RAM	WHITE 3

1 Calibration may be affected if the output amplifier boards are interchanged.

2 Delay and width must be recalibrated if the delay and width board are interchanged or if the scratch-pad RAM board is replaced.

3 The white ejector boards are position interchangeable.

SECTION 6
CALIBRATION

6.1 FACTORY REPAIR

Wavetek maintains a Customer Service department for those customers not possessing the necessary personnel or test equipment to maintain their instrument. If an instrument is returned to Wavetek for repair or calibration, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 CALIBRATION

The following calibration procedure is used to totally align the 859 or used to calibrate individual boards. Individual procedures would be used in the case of a circuit board replacement, repair or for out-of-spec operation of a particular board.

> *NOTE*
>
> *The completion of the calibration procedure returns the instrument to correct alignment.*
>
> ***CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS***
>
> *Instrument specifications are given in Section 1 of this manual.*

Periodic calibration of all boards is needed because of component aging, which depends on instrument on-time and environment. Use six months as an initial calibration period. If possible keep records of the parameter values, see Tables 2-5, 2-6 and 2-7 and increase the time between calibrations if the records indicate.

The boards are shown in Figure 6-1 with a listing and location of individual board assemblies. For access to the board assemblies remove the four screws securing the top cover and lift the cover off the instrument.

> **CAUTION**
>
> Interchanging of "identical" boards throws the instrument out of alignment. Recalibration will be required.

Extender boards are available from Wavetek for use in calibration and repair of the 859. While the majority of boards may be calibrated without extender boards, it is recommended that the delay-and-width and output amplifier boards be calibrated on extender boards and that extender boards be used for access to mother board test points. Part number for the extender boards are listed in paragraph 6.3, Recommended Test Equipment and Accessories.

The calibration procedures included in this section are:

Procedure	Paragraph
Low Amp (Current) Power Supply	6.4
Hi Amp (Current) Power Supply	6.5
Display Logic	6.6
Clock Oscillator	6.7
Delay and Width	6.8
Output Amplifier	6.9

Table 2-5 provides a performance test procedure for verifying the calibration accuracy. Tables 2-6 and 2-7 can be duplicated and used as records for the performance test procedure.

The air inlet for the instrument cooling fan contains a filtering screen that must be cleaned periodically. To clean, remove the screen retainer and screen (at the rear of the instrument). Vacuum or wash and dry the screen as necessary.

6.3 RECOMMENDED TEST EQUIPMENT AND ACCESSORIES

The following test equipment and accessories are recommended for calibration of the 859:

Oscilloscope, Main Frame	Tektronix 7900 Series
Sampling Plug-in for Scope	Tektronix 7S14
Digital Voltmeter	Fluke 8502A
Counter	Hewlett-Packard 5370A
Time Interval Probes	Hewlett-Packard 5363B
Coax Cables	Tektronix 012-0057-01
50Ω Terminator	Narda 376 BNM 50Ω 40W
Oscilloscope	Tektronix 475
Oscilloscope Probes	Tektronix P6106
50°C Test Environment Extender Boards:	
A	Wavetek 1100-00-0692
B	Wavetek 1100-00-0799
C	Wavetek 1100-00-0517

6.4 LOW AMP (CURRENT) POWER SUPPLY

The low current power supply contains all the test points and adjustments for +15V, −15V, isolated +5V and the floating supplies for channels 1 and 2: floating +15V, −15V and +35V.

NOTE

Before verifying, adjusting or attempting any calibration procedure of fault isolation, the power supplies, the voltage card and fuse should be checked; see paragraph 2.2.1.

Refer to table 6-1 for the low amp (current) power supply calibration procedure. All test points and adjustments are located on the circuit board. Test points and adjustments are on the top edge of the board and clearly labeled.

6.5 HIGH AMP (CURRENT) POWER SUPPLY

The high current power supply contains the adjustments for the +5V and −2V supplies and circuitry for the −5.2V supply.

The test points for the +5V logic supply are located on the mother board at J2 (microprocessor board connector). Test points for −2V and −5.2V supplies are located on the mother board at J6 (triggered burst counter board connector). Use extender boards for best access to these test points.

NOTE

Before verifyng, adjusting or attempting any calibration procedure of fault isolation, the power supplies, the voltage card and fuse should be checked; see paragraph 2.2.1.

Refer to table 6-2 for the high current power supply calibration procedure. Test points and adjustments are shown in figures 6-2 and 6-3.

6.6 DISPLAY LOGIC

R5 is adjusted for the loudest beep while repeatedly pressing any front panel key. Refer to table 6-3 for calibration procedure. R5 is clearly visible on the upper edge of the board.

6.7 CLOCK OSCILLATOR

The clock oscillator controls the internal repetition rate of the 859. All calibration adjustments and test points are located on the clock oscillator board.

Refer to table 6-4 for the calibration procedure. Test points are clearly marked on the top edge of the board. Access to adjustable components is through holes in their shielding; the access holes are labeled at the top edge of the board.

6.8 TRIGGER AND BURST COUNTER

The Trigger and Burst Counter board contains the circuitry for the sync and clock outputs. All calibration adjustments are located on the trigger and burst counter board.

Refer to table 6-5 for calibration procedure and figure 6-6 for adjustment locations.

6.9 DELAY AND WIDTH

Delay and width test points adjustments are located on the piggyback portion of the delay-and-width board and on the scratch-pad RAM board. If the 859 has the optional second channel, there will be two delay and width boards. The test points and adjustments are visible and accessible when the boards are in their normal position.

The delay-and-width board requires two calibration adjustments at 50°C. If a 50°C environment is unavailable, a simpler procedure may be used. Place test cover, with two holes to allow access to R63 and R68, on the instrument and allow the instrument to warm up for an hour. After the warmup period, the adjustments are made. This procedure compensates for a 15°C internal temperature rise. When calibrated in a 50°C environment, the compensation is for a 25°C internal temperature rise.

Refer to table 6-6 for the calibration procedure.

6.10 OUTPUT AMPLIFIER

The output amplifier contains circuitry controlling output levels and transitions times. All test points and calibration adjustments are located on the output amplifier board. An extender is required for adjustment access. If the 859 has the optional second channel, there will be two output amplifier boards to calibrate.

The output levels are calibrated for a 50Ω precision load. If a precision 50Ω load is unavailable for calibration, use the following procedures to determine voltages that should be measured when calibrating.

Measure the resistance of the external load (R) and key into the 859 the voltage required in the calibration procedure ($V_{procedure}$). Calibrate the 859 for this voltage at the load:

$$\text{Voltage at Load} = V_{procedure}\left(\frac{2R}{50+R}\right)$$

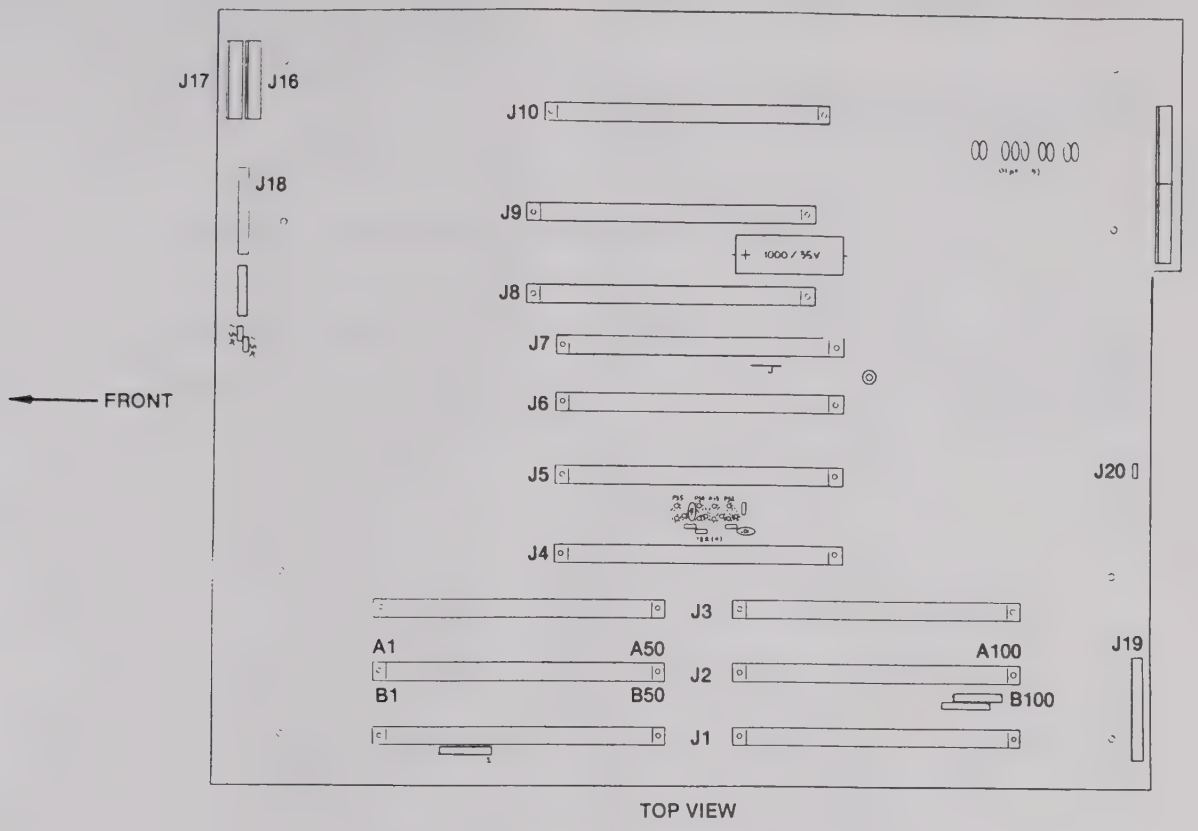


Figure 6-2. Mother Board Connectors

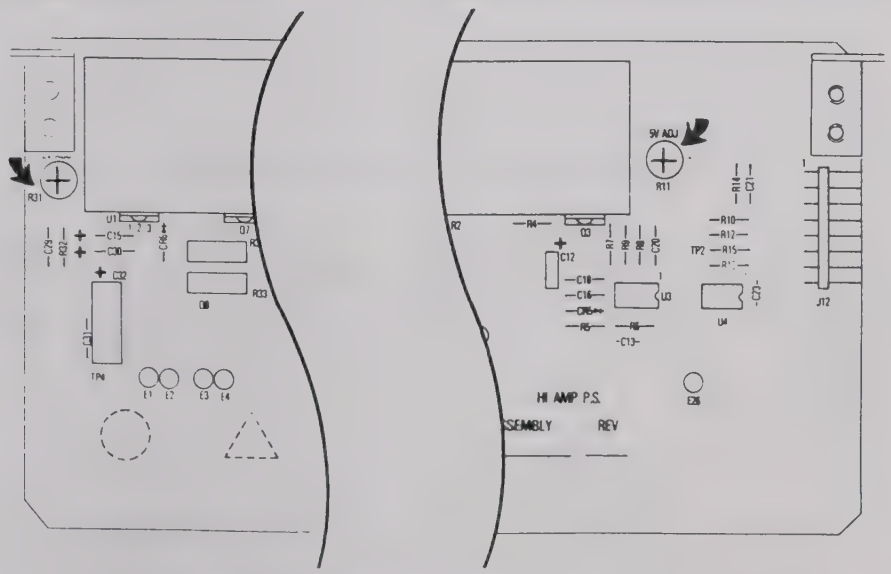


Figure 6-3. Hi Amp (Current) Power Supply Calibration

For example, table 6-7, step 24, asks for 10V into a precision 5Ω load and 10V would be keyed into the 859. Say that the load used was actually 45Ω, then R76 (ref: step 24) would be adjusted until the channel output was not 10V, but

$$\text{Voltage at Load} = 10\text{V}\left(\frac{2[45]}{50+45}\right) = 9.47\text{V}$$

Refer to table 6-7 for the output amplifier calibration procedure. Test points and adjustments are shown in figure 6-7.

Table 6-1. Low Amp (Current) Power Supply Calibration

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	Channel 1 F^{-15}	DVM (dc mode)	TP13 (F ground) TP3	Power: On (Initial power-up settings)	R21	−15 ±0.05 Vdc	All test points and adjustments are loacted on the amp power supply board
2	Channel 1 F_{+15}		TP13, TP1		R20	+15 ±0.05 Vdc	
3	Channel 1 F^{+35}		TP13, TP12		R53	+35 ±.1 Vdc	
4	Channel 2 F^{-15}		TP15 (F ground), TP6		R25	−15 ±.05 Vdc	
5	Channel 2 F^{+15}		TP15, TP4		R24	+15 ±.05 Vdc	
6	Channel 2 F^{+35}		TP15, TP14		R54	+35 ±.1 Vdc	
7	+15		TP8, TP7		R37	+15 ±.05 Vdc	
8	−15V		TP8, TP9		None	−15 ±.1 Vdc	Verify
9	ISO +5V		TP11, TP10			+5 ±.2Vdc	

Table 6-2. High Amp (Current) Power Supply Calibration

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	+5V	DVM (dc mode)	J2-A1 (ground), J2-A50	Power: On (Initial power up settings).	R11	+5 ±.05 Vdc	All test points are located on the mother board and accessible on the extender board. Adjustments are located on the hi amp power supply board
2	−2V		J6-A35 (ground), J6-A43.		R31	−2 ±.05 Vdc	
3	−5.2V		J6-A35, J6-A41		None	−5.2 ± .2 Vdc	Verify

Table 6-3. Display Calibration

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	Keyboard Beeper Frequency Adjust			Repeatedly press any key on front panel	R5	Loud beep	Adjust for loudest beep while repeatedly pressing front panel key

Table 6-4. Clock Oscillator Calibration

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	Offset Adjust	DVM (dc mode)	DVM high input to TP-2, low input to TP3	MODE: B0 FUNC: C2 LE: U4E-9 TE: V4E-9 UL: A.5 LL: D – .5 NORM/COMP: O0 OUTPUT: P1 FREQ: F25E6	R39	0 ± .005 Vdc	Remove cover to shielded circuit. Move jumper from E1 and E2 to between E2 and E3
2							Move Jumpers: From E2 and E3 to between E1 and E2
3	– 4.5V		DVM high input to TP-5		R42	– 4 5 ± .01 Vdc	
4	25 MHz Symmetry	Scope (5 ns/div)	DVM high input to TP-6		R24	Symmetrical Output. 20 ± .2ns on each ½ cycle (25 MHz ± 250 kHz)	Connect Scope probes to TP6 and circuit ground.
5	First Pulse Width	Scope (figure 6-4). External	CH 1 OUT	MODE: B2 (gate) TRIG FORMT: K0	R15	1st pulse period same as other pulses. Minimum delay between CH 1 and sync	Externally trigger at 5 MHz rate.
6	25 MHz Frequency	Time Interval Probes and Counter (figure 6-5)		MODE: B0	R11	25 ± .05 MHz	
7	50 MHz Frequency			FREQ: F50E6	R37	50 ± .05 MHz	Repeat steps 6 and 7, if necessary. Replace cover and proceed

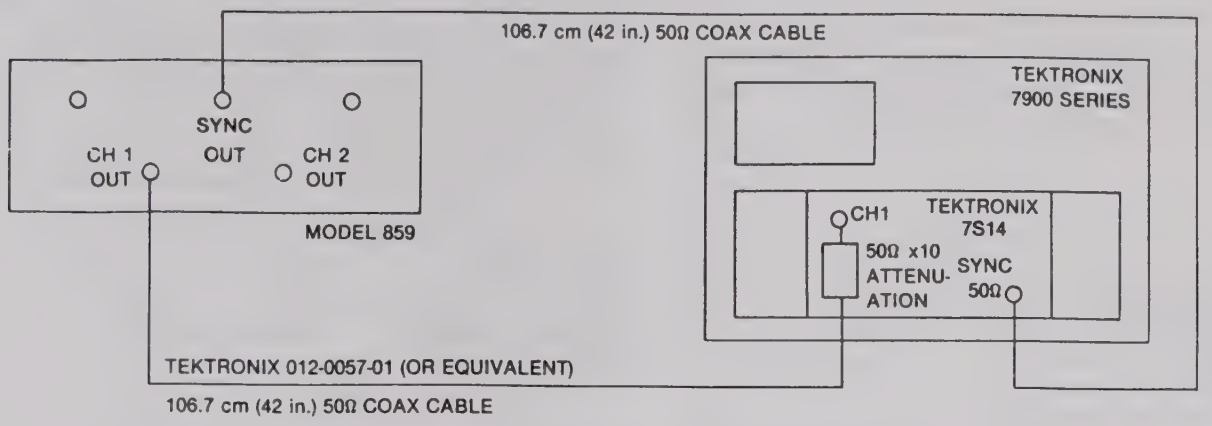


Figure 6-4. Model 859 / Oscilloscope Calibration Setup

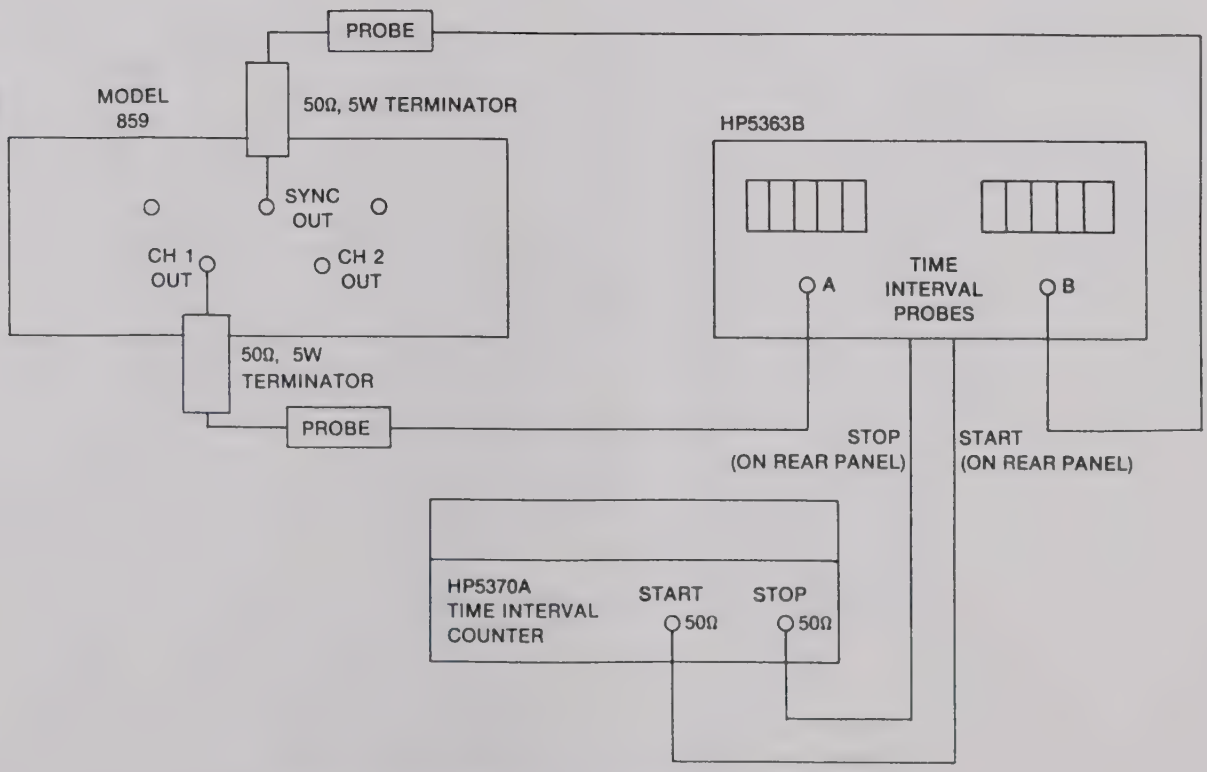


Figure 6-5. Model 859/Time Interval Probes and Counter Calibration Setup

Table 6-5. Trigger and Burst Counter Calibration

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	Sync Drive	Scope	SYNC OUT (50Ω load)	MODE: B0	R64	Symmetrical Output 10 ±.1 ns on each ½ cycle	Set scope for 5 ns/div sweep
2	Clock Drive		CLOCK OUT (50Ω load)		R16		
3	Manual Sync Drive	Scope, External Signal	SYNC OUT (50Ω load) FREQ: 25E6	MODE: B2 TRIG FORMT: K0 Center TRIGGER LEVEL Control (rear panel)	R60	Symmetrical Output. 10 ± .2 ns on each ½ cycle	Trigger input from signal source: ±4V peak, triangle at 50 MHz rate. Set scope for 20 ns/div sweep. Center 859 trigger level control (on rear panel).

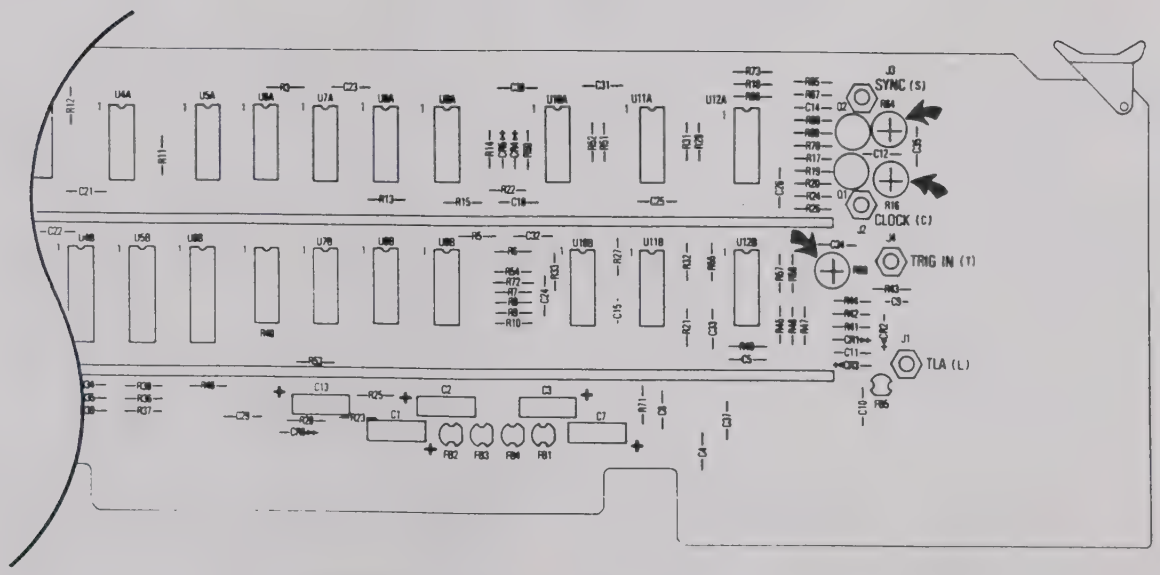


Figure 6-6. Trigger and Burst Counter Calibration

Table 6-6. Delay and Width Channel 1 (and 2) Calibration

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	16 ns Delay	Scope or time Interval Probes and Counter (figure 6-4 or 6.5)	CH 1 OUT	Scratch Pad RAM Bd: Set the 8 switches to 0. MODE: B0 FUNC: C0 FREQ: F10E6 UL: A.5 LL: D – .5 NORM/COMP: O0 OFF/ON: P1 LE: U4E-9 TE: V4E-9 DELAY: L15E-9 then 16E-9	C2	1 ns change as delay is varied from 15 ns to 16 ns	Adjust C2 for 1 ns change as delay is increases 1 ns
2	28 ns Width			Delay: L0 Width: N28E-9 then 29E-9	C23	1 ns change as width is varied from 28 ns to 29 ns	Adjust C23 for 1 ns change as width is increased 1 ns
3	0 ns Delay Compensation			DELAY: L0	Scratch Pad SW 1 for CH 1 (SW 5 for CH 2)	Lowest delay setting between SYNC OUT and CH 1 OUT (CH 2 OUT) (Less then 2 ns)	After each change in switch position, reprogram DELAY: 0 and Exec. Select the switch position with minimum delay between channel and Sync Outputs.
4	10 ns Width Compensation			WIDTH: N10E-9	Scratch Pad SW 3 for CH 1. SW 7 for CH 2)	10 ± .5 ns width	Measure between 50% point of leading edge and trailing edge. After each change in switch position, reprogram WIDTH: N10E-9 EXEC.
5	Delay Counter Compen-			DELAY: L24E-9 then 25E-9	Scratch Pad SW 2 for CH 1 (SW 6 for CH 2)	1 ± .5 ns delay increase	Adjust switch for 1 ns increase in delay, with respect to SYNC OUT, as delay is increased 1 ns. After each change in switch position, reprogram DELAY: 24E-9 Exec. then DELAY 25E-9 Exec.
6	Width Counter Compensation			WIDTH: N34E-9 then 35E-9 DELAY: L0	Scratch Pad SW 4 for CH 1 (SW 8 for CH 2)	1 ± .5 ns width increase	Adjust switch for 1 ns increase in width, measured at 50% point of leading edge to trailing edge, as width is increased 1 ns. After each switch position change, reprogram WIDTH: 34-9 and Exec then 35E-9 and Exec.
7	25°C Zero Balance	DVM (dc mode)	Circuit ground, TP1	FREQ: F4E2 DELAY: L999E-6 WIDTH: N999E-6	R56	0 ± .05 Vdc	
8	4V Width		Circuit ground, TP2		R59	+4 Vdc ± .1V	

Table 6-6. Delay and Width Channel 1 (and 2) Calibration (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
9	4V Delay		Circuit ground, TP3		R67	+4 ±.1 Vdc	
10	Delay	Time Interval Probes and Counter (figure 6-5)	CH1 OUT (CH 2 OUT)		C3	999 ±1μs	Delay at channel output with respect to SYNC OUT
11	Width				C22	999 ±1μs	Pulse width measured at 50% points between leading edge and trailing edge
12	50°C Width				R63	999 ±1μs	Place 859 in 50°C environment allow 1 hour warm-up. Pulse width measured at 50% points between leading edge and trailing edge. See paragraph 6.9 for alternate method.
13	50°C Delay				R68	999 ±1μs	Place 859 in a 50°C environment allow 1 hour warm-up. Pulse delay measured at channel output relative to SYNC OUT. See paragraph 6.9 for alternate method.
14							Repeat steps 1 through 13 for second channel if applicable.

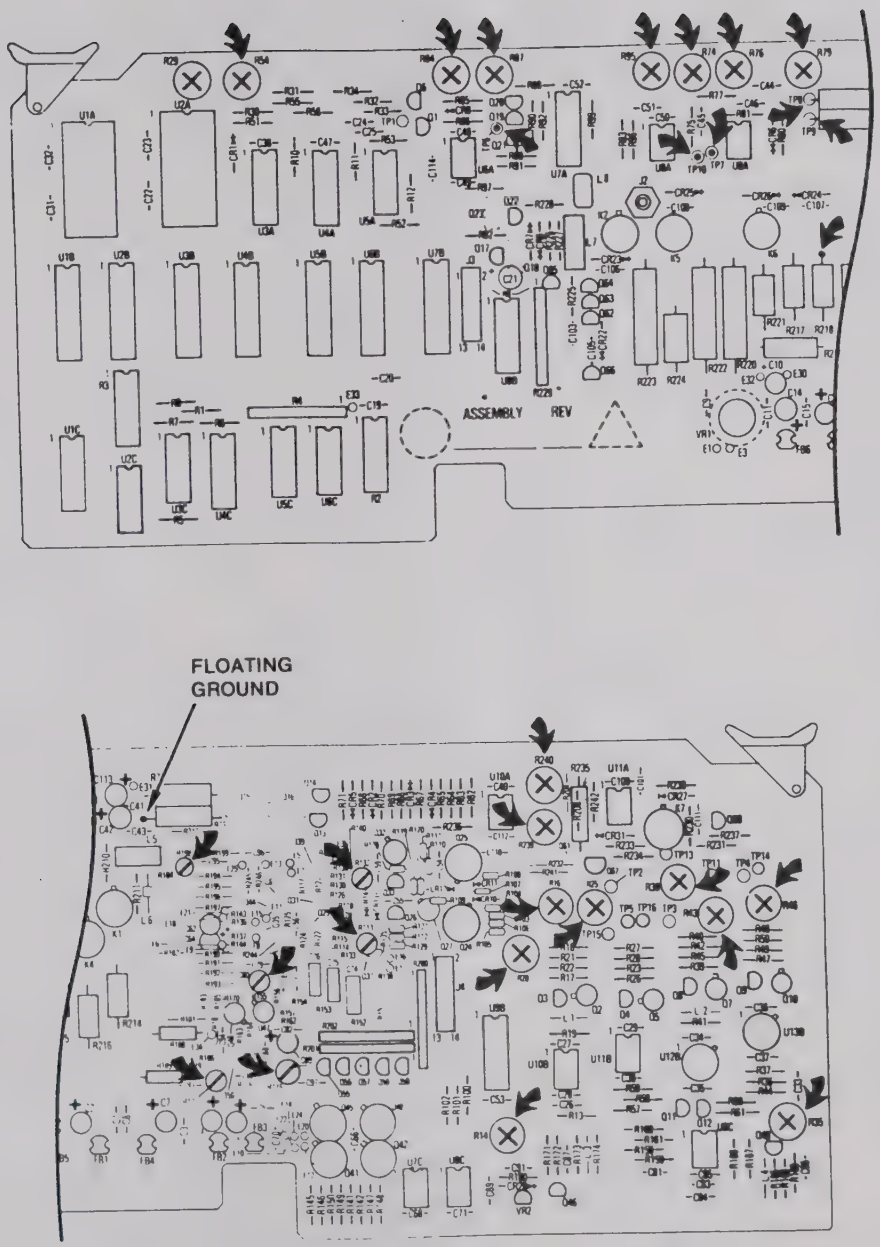


Figure 6-7. Output Amplifier Calibration

Table 6-7. Power Amplifier Channel 1 (and 2) Calibration

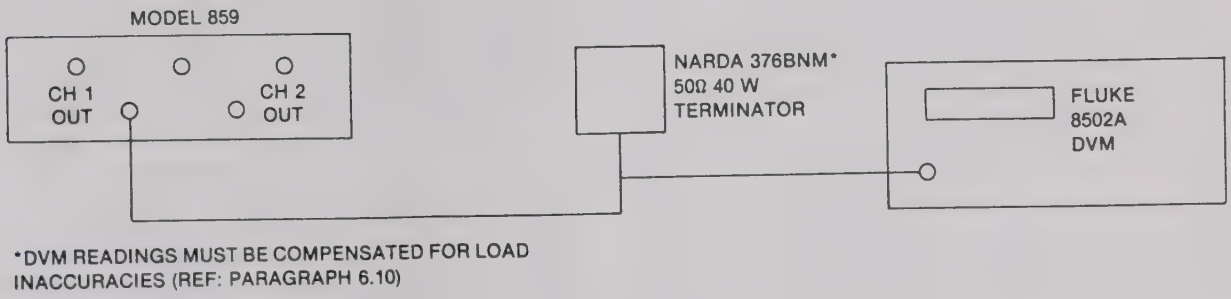
Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
1	Upper Level step	Scope	CH OUT	MODE: B0 FUNC: C2 FREQ: F5E6 UL: A0 LL: D – 10 LE: U4E-9 TE: V50E-9 OFF/ON: P1 NORM/COMP: O0	R132	Minimum step at corner of upper level and trailing edge	Adjust to minimize step without affecting upper level
2	Lower Level step			LE: U50E-9 TE: V4E-9	R113	Minimum step at corner at lower level and leading edge	Adjust to minimize step without affecting the lower level
3	Trailing Edge	Time Interval Counter and (figure 6-5)		LE: U5E-6 TE: V5E-6 FREQ: F5E2	R14	5 ± .01μs	Set time interval counter trigger levels. Start probe A: – 1.00V negative going pulse Stop probe A: – 9.00V negative going pulse
4	Leading Edge				R35	Set time interval	Start probe A: – 9.00V positive going pluse, Stop probe A: – 1.00V positive going pulse.
5	Leading Edge Zero			LE: U500E-6 TE: V5E-6	R38	500 ± 1μs	
6	Trailing Edge zero			LE: U5E-6 TE: V500E-6	R16		Set time interval counter trigger levels. Start probe A: 1 – 100V negative going pulse, Stop probe A: – 9.00V negative going pulse. Repeat steps 3 through 6 as necessary
7	50 ns Range			LE: U250E-9 TE: V250E-9	C80	250 + 1ns	Set time interval counter trigger level. Stop probe A: – 1.00V positive going pulse, Start probe A: – 9.00V positive going pulse
8	Trailing Edge			LE: U49.9E-9 TE: V49.9E-9	R20	49.9 ± .1ns	
9	Leading Edge				R43		
10	Leading Edge Comp-sation	DVM (dc mode) (figure 6-8)		LE: U49.9E-9 TE: V49.9E-9 MODE: B4 NORM/COMP: O1		Measure output level	Read instructions for steps 10 and 11 completely before making any adjustments.

Table 6-7. Power Amplifier Channel 1 (and 2) Calibration (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
11				LE: U4E-9	R46	Set R46 equal to measured output of step 10 ± 10 mV.	
12	Trailing Edge Comp-sation			LE: U49.9E-9 TE: V49.9E-9 MODE: B4 NORM/COMP: O0		Measure output level	Read instructions for steps 12 and 13 completely before making any adjustments.
13				TE: V4E-9	R25	Set R25 to equal measured output of step 12 ± 10 mV	
14	Offset Balance		F. ground and TP6	UL: A0 LL: D – 10 TRIG FORMT: K2 NORM/COMP: O1 LE: U4E-9 TE: V4E-9	R84	0 ± 1 mVdc	1. Adjust R84 for a positive voltage, approximately + 10 mV 2. Adjust R84 until voltage at TP6 reaches 0V ± 1 mV. NOTE: It is important to stop rotating R84 at zero volts. Further rotation results in improper calibration
15	Negative Offset Zero	DVM (dc mode)	TP9 (ground) and TP10	UL: A – .1	R95	0 ± 1 mV	
16	Positive Offset Zero		TP7 (ground) and TP8	UL: A.1	R79	0 ± 1 mV	
17	Output Zero		CH OUT	UL: A0 LL: D – 10	R239	0 ± 10 mV	CH OUT terminated into 42 in. of RG58 coax with a 50Ω load
18	Negative Offset			UL: A – 9.9 LL: D – 10	R87	– 9.90 ± .01V	
19	Positive Offset			UL: A10 LL: D0	R76	+ 10V ± 10 mV	See paragraph 6.10 for load inaccuracy compensation.
20	Amplitude			UL: A10 LL: D0 NORM/COMP: O0	R54	0V ± 10 mV	
21	Amplitude Compensation			UL: A10 LL: D5.01 NORM/COMP:O1	R240	10 ± .01V	
22	F supply	DVM (dc mode)	DVM low to top of R218. DVM high to F (ground)	UL: A10 LL: D0	R74	– 10V ± .01V	Disconnect all cables from 859 before making this adjustment.

Table 6-7. Power Amplifier Channel 1 (and 2) Calibration (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
23	Fast Peaking	Sampling Scope (figure 6-4)	CH OUT	FREQ: F12E6 LE: U4E-9 TE: V4E-9 UL: A0 LL: D-10 MODE: B0	R175	Best waveform quality without causing leading or trailing edges to be greater then 4.8 ns	
24	Slow Peaking				R198		
25	Bandwidth				R177		
26	Second Channel						For Second Channel: Repeat steps 1 through 25



*DVM READINGS MUST BE COMPENSATED FOR LOAD INACCURACIES (REF: PARAGRAPH 6.10)

Figure 6-8. Model 859/DVM Calibration Setup

SECTION 7

PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown below.

7.2 ADDENDA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, addendum pages are prepared to summarize the changes made and are inserted immediately inside the rear cover. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

Revision levels located on parts lists and drawings are completely independent and are likely to be different within any assembly.

DRAWING	DRAWING NUMBER	
Instrument Schematic	0004-00-0147	
Chassis Assembly	0102-00-0670	(Sheets 1 and 2 of 3 only)
Chassis Parts Lists	1101-00-0670	
Display Logic Schematic	0103-00-0690	
Display Logic Assembly	1100-00-0690	
Display Logic Parts List	1100-00-0690	
Front Panel Assembly	0102-00-0671	
Front Panel Parts List	1101-00-0671	
Rear Panel Assembly	0102-00-0672	
Rear Panel Parts List	1101-00-0672	
Mother Board Schematic	0103-00-0702	
Mother Board Assembly	1100-00-0702	
Mother Board Parts List	1100-00-0702	
Hi Amp (Current) Power Supply Schematic	0103-00-0701	
Hi Amp (Current) Power Supply Assembly	1100-00-0701	
Hi Amp (Current) Power Supply Assembly	0101-00-0701	(Sheet 1 of 2 only)
Hi Amp (Current) Power Supply Parts List	1100-00-0701	
Low Amp (Current) Power Supply Schematic	0103-00-0700	
Low Amp (Current) Power Supply Assembly	1100-00-0700	
Low Amp (Current) Power Supply Parts List	1100-00-0700	

DRAWING	DRAWING NUMBER	
Output Amplifier Schematic	0103-00-0698	
Output Amplifier Assembly	1100-00-0698	
Output Amplifier Board Assembly	0101-00-0698	(Sheet 3 of 3 only)
Output Amplifier Parts List	1100-00-0698	
Piggyback Module Assembly and Parts List	1208-00-1133	
Clock Oscillator Schematic	0103-00-0693	
Clock Oscillator Assembly	1100-00-0693	
Clock Oscillator Parts List	1100-00-0693	
Trigger and Burst Counter Schematic	0103-00-0687	
Trigger and Burst Counter Assembly	1100-00-0687	
Trigger and Burst Counter Parts List	1100-00-0687	
Delay and Width Schematic	0103-00-0694	
Delay and Width Assembly	1100-00-0694	
Delay and Width Parts List	1100-00-0694	
Delay and Width Piggyback Assembly	1208-00-0697	
Delay and Width Piggyback Parts List	1208-00-0697	
Scratch Pad RAM Schematic	0103-00-0688	
Scratch Pad RAM Assembly	1100-00-0688	
Scratch Pad RAM Parts List	1100-00-0688	
Microprocessor Schematic	0103-00-1317	
Microprocessor Assembly	1100-00-1317	
Microprocessor Parts List	1100-00-1317	
GPIB Interface Schematic	0103-00-0685	
GPIB Interface Assembly	1100-00-0685	
GPIB Interface Parts List	1100-00-0685	
GPIB Address Assembly	0101-00-0730	
GPIB Address Parts List	1208-00-0730	

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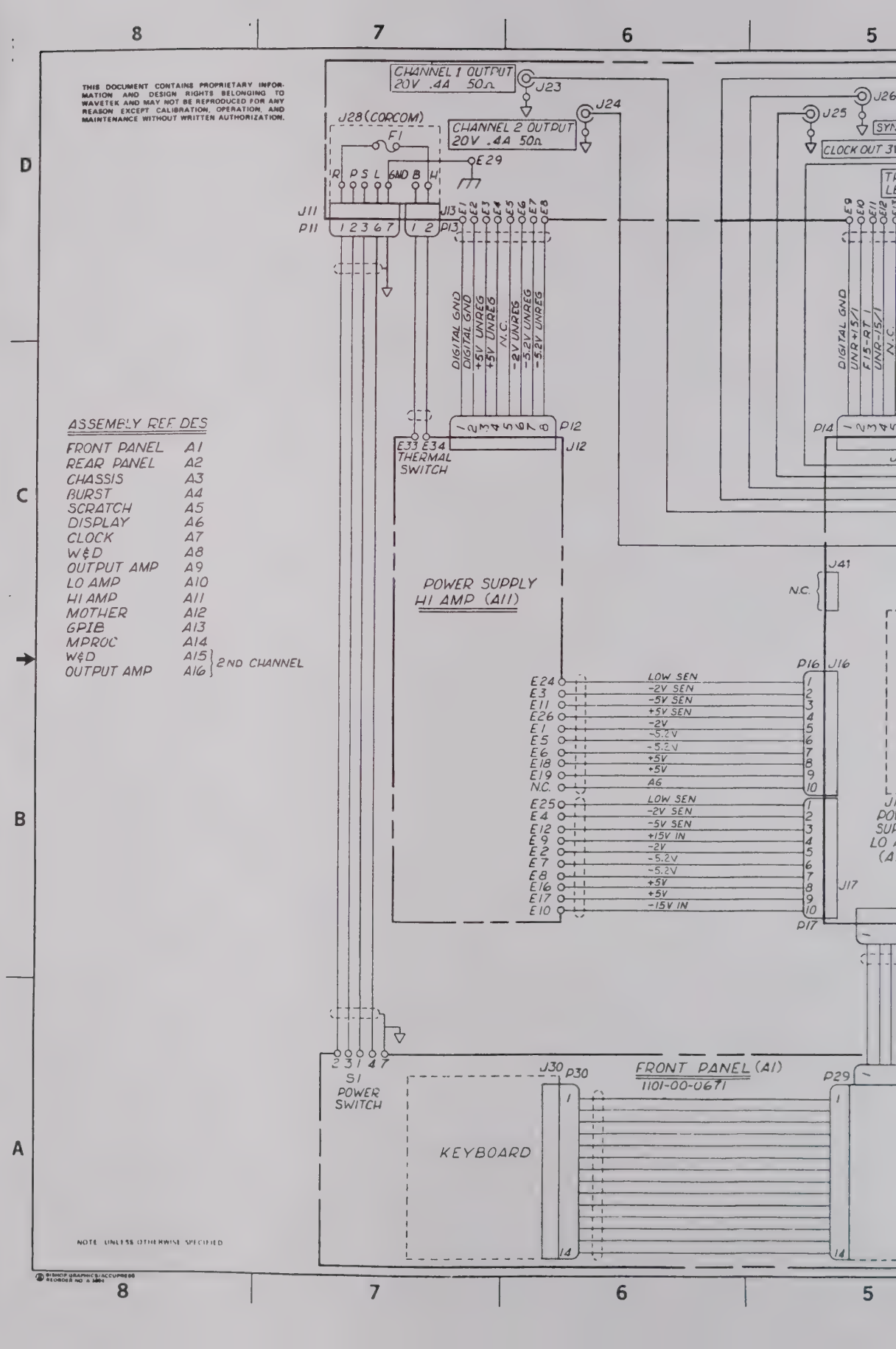
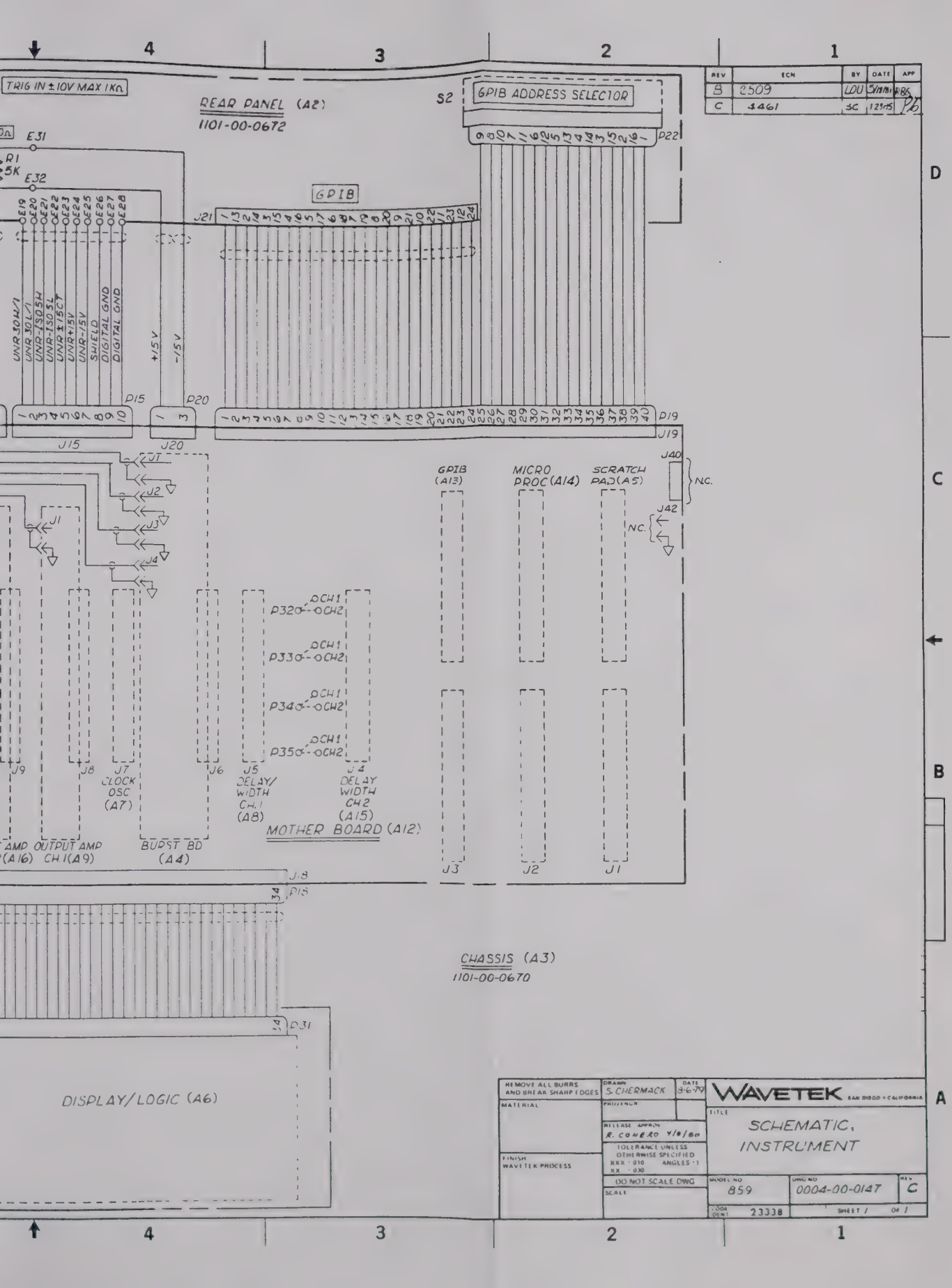


ASSEMBLY	REF DES	
FRONT PANEL	A1	
REAR PANEL	A2	
CHASSIS	A3	
BURST	A4	
SCRATCH	A5	
DISPLAY	A6	
CLOCK	A7	
W&D	A8	
OUTPUT AMP	A9	
LO AMP	A10	
HI AMP	A11	
MOTHER	A12	
GPIB	A13	
MPROC	A14	
W&D	A15	2ND CHANNEL
OUTPUT AMP	A16	2ND CHANNEL

NOTE UNLESS OTHERWISE SPECIFIED



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C | 4461 | SC | 12/3/85 | PB
TRIG IN ±10V MAX 1KΩ
REAR PANEL (A2)
1101-00-0672
S2
GPIB ADDRESS SELECTOR
P22
E31
E32
GPIB
J21
UNR30H/1
UNR30L/1
UNR-ISO5H
UNR-ISO5L
UNR±15CT
UNR+15V
UNR-15V
SHIELD
DIGITAL GND
DIGITAL GND
+15V
-15V
P15
P20
P19
J15
J20
J19
J40
N.C.
J42
N.C.
GPIB (A13)
MICRO PROC (A14)
SCRATCH PAD (A5)
J1
J2
J3
J4
P32
P33
P34
P35
CH1
CH2
J9
J8
J7 CLOCK OSC (A7)
J6
J5 DELAY/ WIDTH CH.1 (A8)
J4 DELAY WIDTH CH2 (A15)
MOTHER BOARD (A12)
AMP (A16)
OUTPUT AMP CH.1 (A9)
BURST BD (A4)
J3
J2
J1
J18
P18
CHASSIS (A3)
1101-00-0670
P31
DISPLAY/LOGIC (A6)
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. CHERMACK
DATE 3-6-79
PROJ ENGR
RELEASE APPROV R. COMERO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC, INSTRUMENT
MODEL NO 859
DWG NO 0004-00-0147
REV C
CODE IDENT 23338
SHEET 1 OF 1

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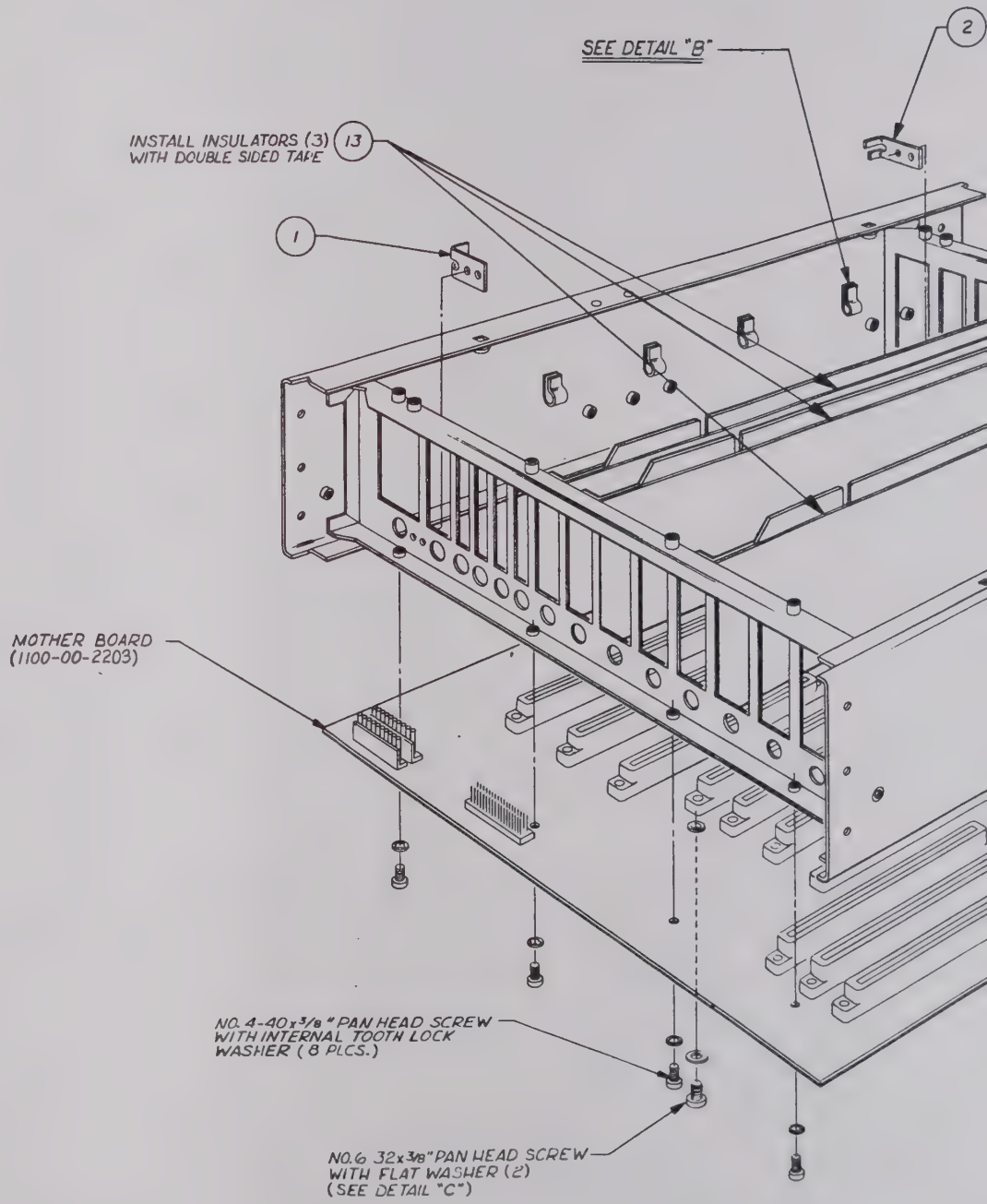

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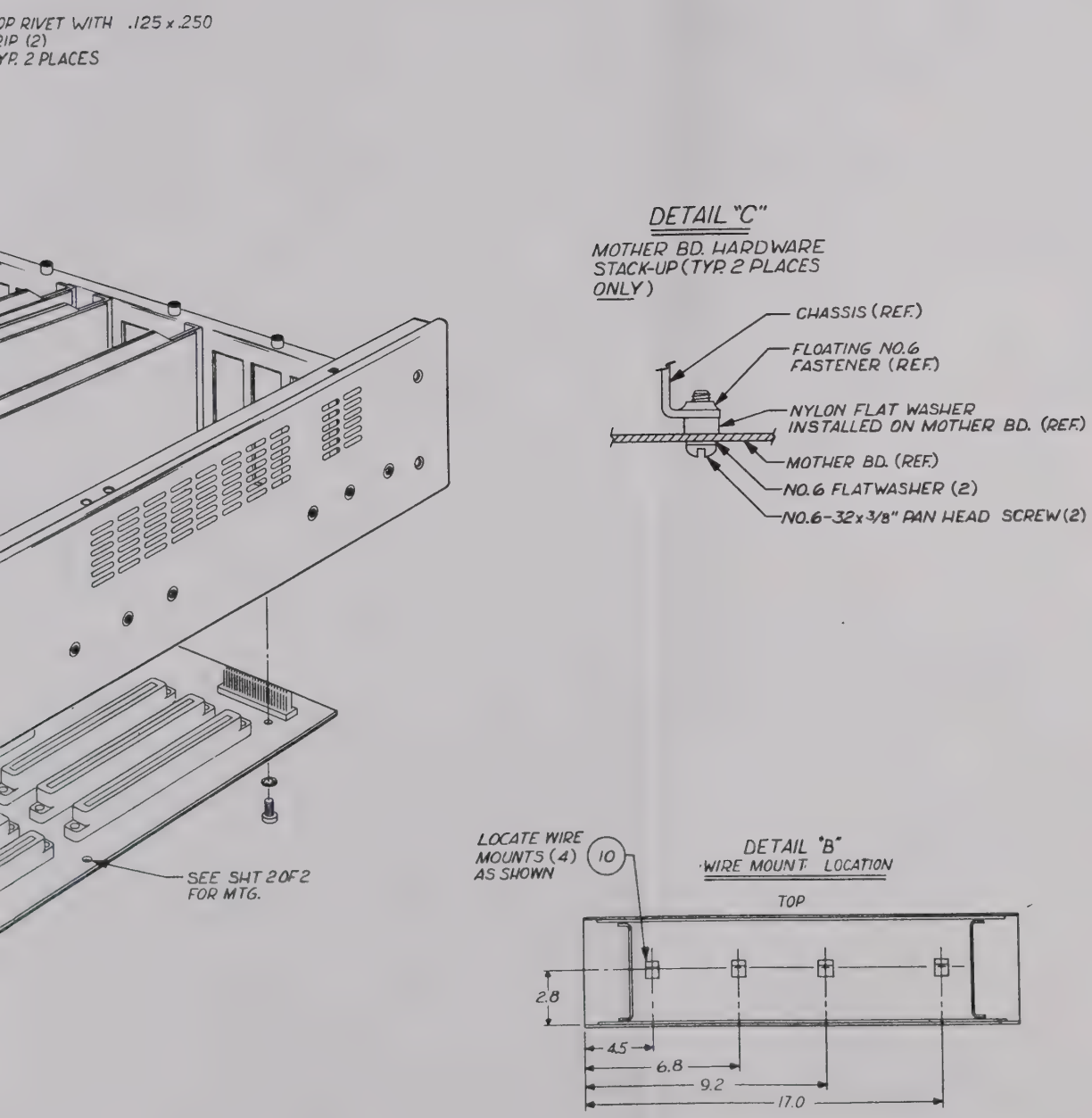
D	#4778	DAM	7/22/[illegible]	[illegible]



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MATERIAL	PROJ ENGR		TITLE ASSEMBLY CHASSIS (A3)
	RELEASE APPROV R. CONERO 4/8/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO 559 / DWG NO 0102-00-0670 / REV D
	SCALE		CODE IDENT 23338 / SHEET 1 OF 3

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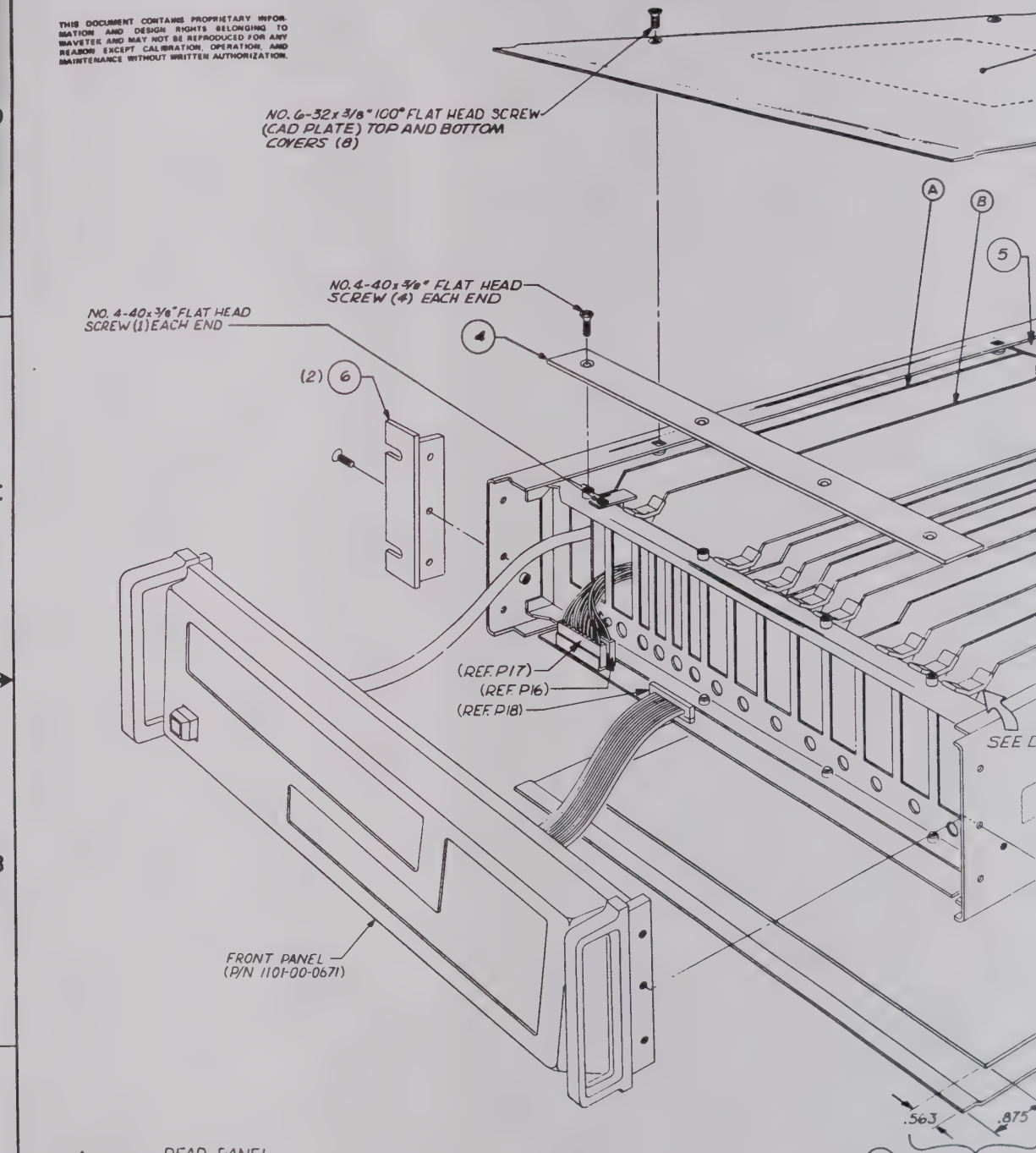
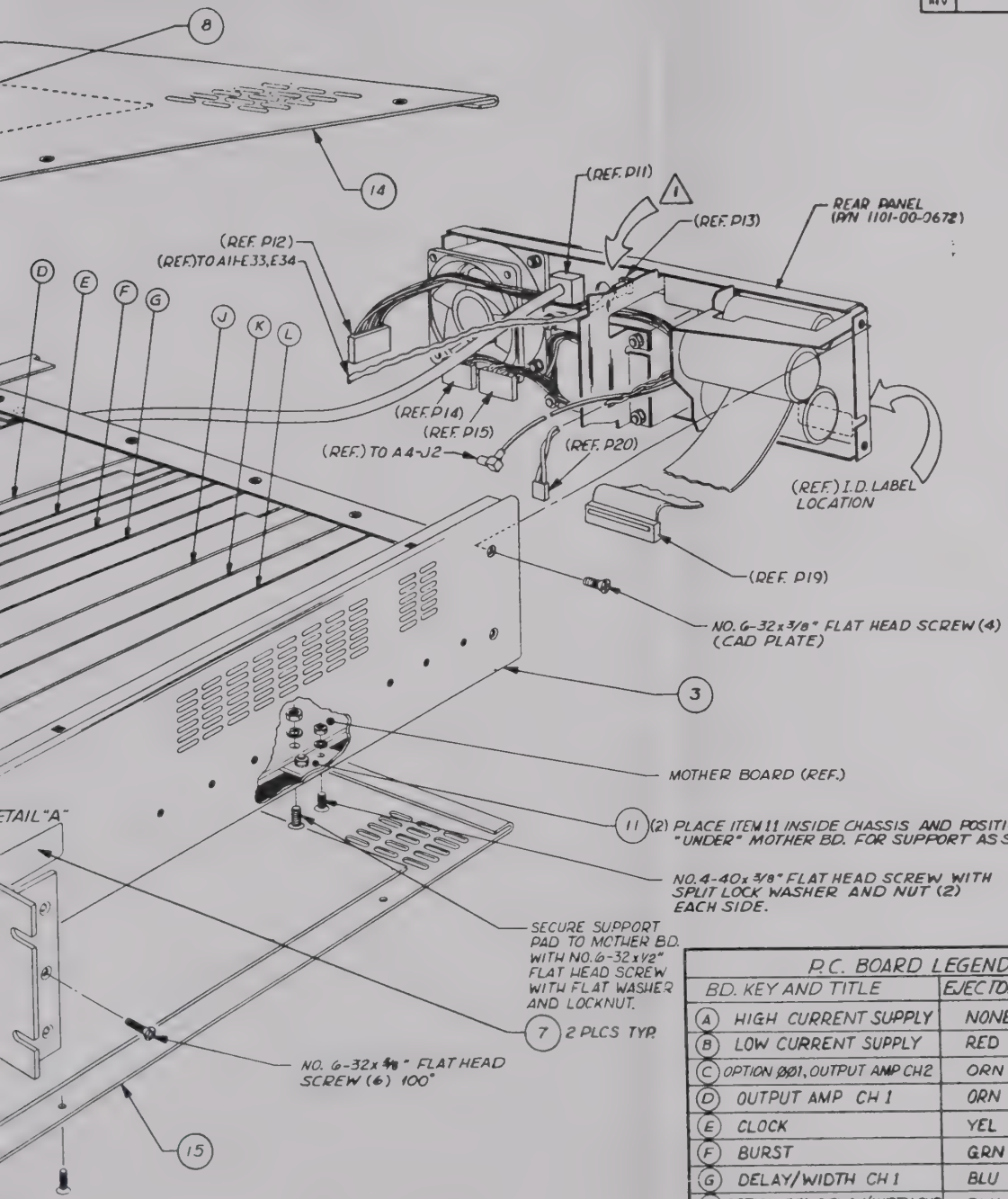


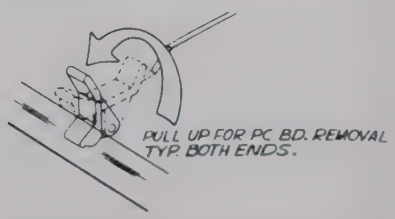
1 REAR PANEL BNC DESTINATION

PANEL FUNCTION	PC. BD. DESTINATION
J27 "TRIG IN"	A4-J4 BURST BD.
J26 "SYNC OUT"	A4-J3 BURST BD.
J25 "CLOCK OUT"	A4-J2 BURST BD.
J23 "CH.1 OUTPUT"	A9-J1 CH.1 OUTPUT AMP.
J24 "CH.2 OUTPUT" (OPTIONAL)	A16-J1 CH.2 OUTPUT AMP. (OPTIONAL)

NOTE UNLESS OTHERWISE SPECIFIED



DETAIL "A"
TYP. PC BD. REMOVAL



P.C. BOARD LEGEND	
BD. KEY AND TITLE	EJECTOR/CARD GUIDE COLOR
(A) HIGH CURRENT SUPPLY	NONE
(B) LOW CURRENT SUPPLY	RED
(C) OPTION Ø01, OUTPUT AMP CH2	ORN
(D) OUTPUT AMP CH 1	ORN
(E) CLOCK	YEL
(F) BURST	GRN
(G) DELAY/WIDTH CH 1	BLU
(H) OPTION Ø01 DELAY/WIDTH CH2	BLU
(J) GPIB	WHT
(K) MICROPROCESSOR	WHT
(L) SCRATCH PAD	WHT

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER 5-7-79
PROJENGR
RELEASE APPROV R COWERD 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
ASSEMBLY CHASSIS (A3)

MODEL NO	DWG NO	REV
859	0102-00-0670	D

CODE IDENT 23338 SHEET 2 OF 3

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REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS	0102-00-0670	WVTK	0102-00-0670	1
6	MTG. BKT	172-6332	WVTK	1400-00-6332	2
13	INSULATOR REF: 3200-03-0001	172-6891	WVTK	1400-00-6891	3
11	SUPPORT PAD	859-9173	WVTK	1400-00-9173	2
1	RETAINER, PC, LH	859-9323	WVTK	1400-00-9323	1
2	RETAINER, PC, RH	859-9333	WVTK	1400-00-9333	1
7	LABEL, REAR SUPPORT	859-0010	WVTK	1400-01-0010	2
3	CHASSIS	115-1772	CALMK	1400-01-0022	1
8	LABEL, PCA GIUDE	859-0430	WVTK	1400-01-0430	1
12	INSULATOR, MOTHER BD	859-1411	WVTK	1400-01-1411	1
4	RETAINER PLATE	859-2013	WVTK	1400-01-2013	1
5	RETAINER PLATE	859-2023	WVTK	1400-01-2023	1
NONE	GUIDE, BOARD	115-287	CALMK	2100-06-0004	6
NONE	CARD GUIDE, RED	115-287 RED	CALMK	2100-06-0008	2
NONE	CARD GUIDE, ORANGE	115-287 ORANGE	CALMK	2100-06-0009	4
NONE	CARD GUIDE, YELLOW	115-287 YELLOW	CALMK	2100-06-0010	2

WAVETEK PARTS LIST	TITLE: CHASSIS	ASSEMBLY NO. 1101-00-0670	REV E
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	CARD GUIDE, GREEN	115-287 GREEN	CALMK	2100-06-0011	2
NONE	CARD GUIDE, BLUE	115-287 BLUE	CALMK	2100-06-0012	4
10	WIRE MOUNT, ADHESIVE	6025-08-BLK	GRAHL	2800-00-0024	4

WAVETEK PARTS LIST	TITLE: CHASSIS	ASSEMBLY NO. 1101-00-0670	REV E
		PAGE 2	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST CHASSIS
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		MODEL NO 859 / DWG NO 1101-00-0670 / REV E
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

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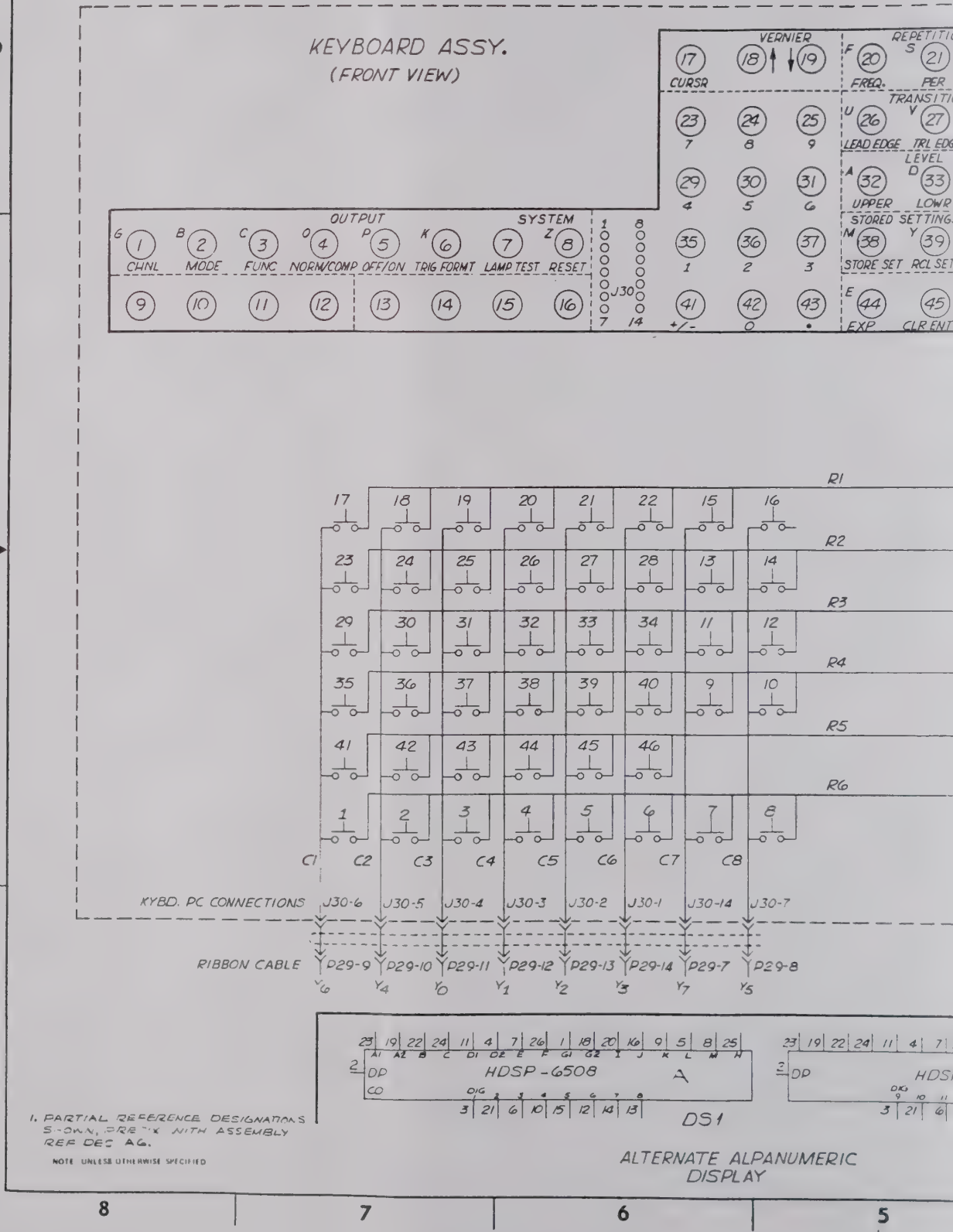

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REF DES A6.

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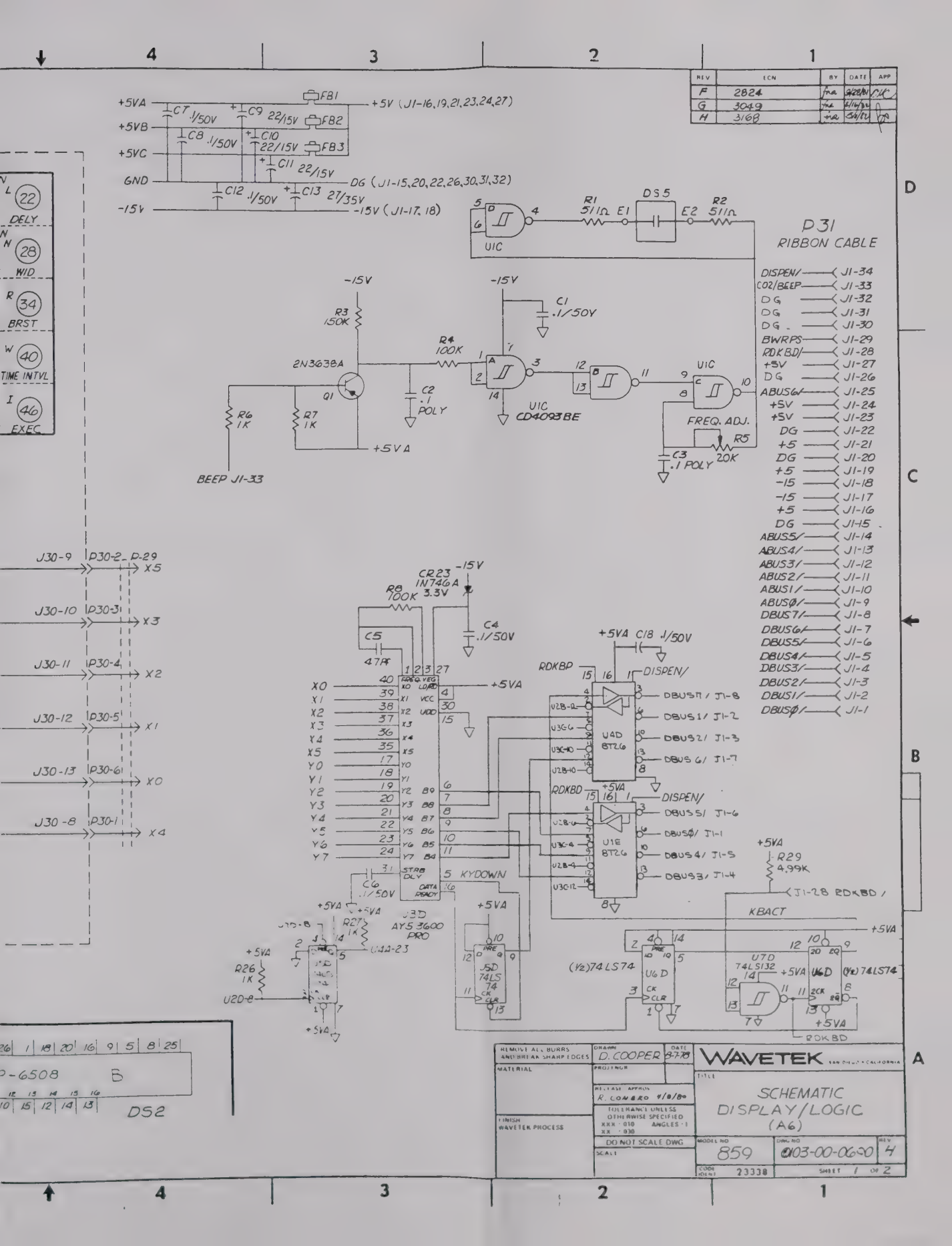
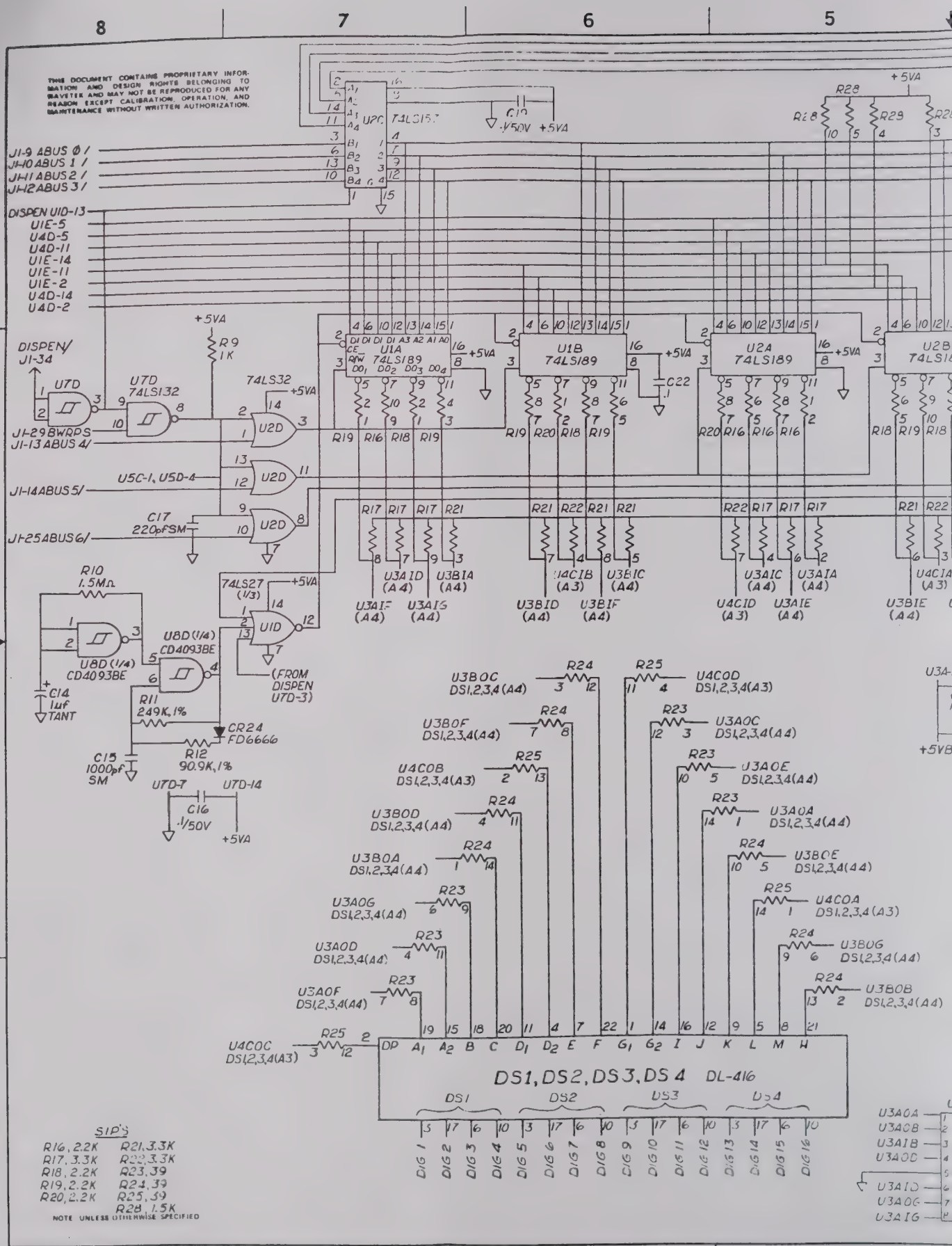


REV | ECN | BY | DATE | APP
F | 2824
G | 3049
H | 3168
+5VA
+5VB
+5VC
GND
-15V
C7 .1/50V
C8 .1/50V
C9 22/15V
C10 22/15V
C11 22/15V
C12 .1/50V
C13 27/35V
FB1
FB2
FB3
+5V (J1-16,19,21,23,24,27)
DG (J1-15,20,22,26,30,31,32)
-15V (J1-17, 18)
DS5
R1 511Ω
R2 511Ω
E1
E2
U1C
P31
RIBBON CABLE
DISPEN/ J1-34
CO2/BEEP J1-33
DG J1-32
DG J1-31
DG J1-30
BWRPS J1-29
RDKBD/ J1-28
+5V J1-27
DG J1-26
ABUS6/ J1-25
+5V J1-24
+5V J1-23
DG J1-22
+5 J1-21
DG J1-20
+5 J1-19
-15 J1-18
-15 J1-17
+5 J1-16
DG J1-15
ABUS5/ J1-14
ABUS4/ J1-13
ABUS3/ J1-12
ABUS2/ J1-11
ABUS1/ J1-10
ABUS0/ J1-9
DBUS7/ J1-8
DBUS6/ J1-7
DBUS5/ J1-6
DBUS4/ J1-5
DBUS3/ J1-4
DBUS2/ J1-3
DBUS1/ J1-2
DBUS0/ J1-1
R3 150K
2N3638A
Q1
R6 1K
R7 1K
BEEP J1-33
R4 100K
C2 .1 POLY
C1 .1/50V
U1C CD4093BE
FREQ. ADJ.
R5 20K
C3 .1 POLY
DELY
WID
BRST
TIME INTVL
EXEC
J30-9 P30-2 P-29 X5
J30-10 P30-3 X3
J30-11 P30-4 X2
J30-12 P30-5 X1
J30-13 P30-6 X0
J30-8 P30-1 X4
CR23 1N746A 3.3V
R8 100K
C4 .1/50V
C5 47PF
C6 .1/50V
U3D AY5 3600 PRO
KYDOWN
RDKBP
RDKBD
U4D 8T26
U1E 8T26
DISPEN/
DBUS7/ J1-8
DBUS1/ J1-2
DBUS2/ J1-3
DBUS6/ J1-7
DBUS5/ J1-6
DBUS0/ J1-1
DBUS4/ J1-5
DBUS3/ J1-4
R29 4.99K
J1-28 RDKBD/
KBACT
U4A-23
R27 1K
R26 1K
U2D-8
U5D 74LS74
(1/2)74LS74
U6D
U7D 74LS132
(1/2)74LS74
RDKBD
P-6508 B
DS2
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER
DATE 8-7-78
PROJ ENGR
RELEASE APPROV R. COMBRO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO CALIFORNIA
TITLE
SCHEMATIC DISPLAY/LOGIC (A6)
MODEL NO 859
DWG NO 0103-00-0600
REV 4
CODE IDENT 23338
SHEET 1 OF 2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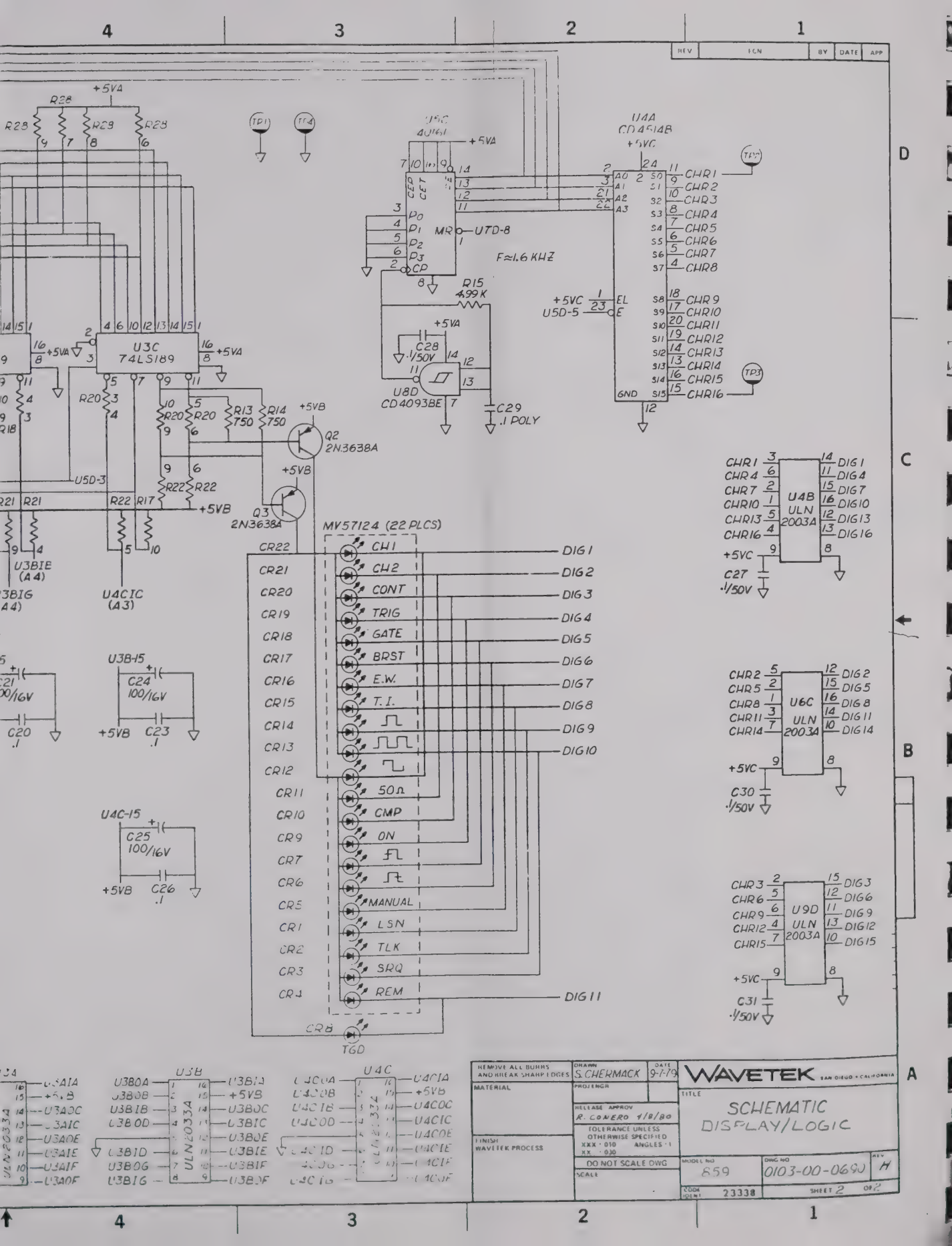
J1-9 ABUS Ø /
J1-10 ABUS 1 /
J1-11 ABUS 2 /
J1-12 ABUS 3 /
DISPEN U1D-13
U1E-5
U4D-5
U4D-11
U1E-14
U1E-11
U1E-2
U4D-14
U4D-2
DISPEN/ J1-34
J1-29 BWRPS
J1-13 ABUS 4/
J1-14 ABUS 5/
J1-25 ABUS 6/
U5C-1, U5D-4
C17 220pf SM
R9 1K
R10 1.5MΩ
C14 1uf TANT
R11 249K, 1%
R12 90.9K, 1%
CR24 FD6666
C15 1000pf SM
C16 .1/50V
U7D-7
U7D-14
(FROM DISPEN U7D-3)
U2C 74LS157
C19 .1/50V
+5VA
U1A 74LS189
U1B 74LS189
U2A 74LS189
U2B 74LS189
C22 .1
U3AID (A4)
U3BIA (A4)
U3AIF (A4)
U3AIG (A4)
U3BID (A4)
U3BIF (A4)
U4CIB (A3)
U3BIC (A4)
U3AIC (A4)
U3AIA (A4)
U4CID (A3)
U3AIE (A4)
U3BIE (A4)
U4CIA (A3)
U3BOC DS1,2,3,4(A4)
U4COD DS1,2,3,4(A3)
U3BOF DS1,2,3,4(A4)
U3AOC DS1,2,3,4(A4)
U4COB DS1,2,3,4(A3)
U3AOE DS1,2,3,4(A4)
U3BOD DS1,2,3,4(A4)
U3AOA DS1,2,3,4(A4)
U3BOA DS1,2,3,4(A4)
U3BOE DS1,2,3,4(A4)
U3AOG DS1,2,3,4(A4)
U4COA DS1,2,3,4(A3)
U3AOD DS1,2,3,4(A4)
U3BOG DS1,2,3,4(A4)
U3AOF DS1,2,3,4(A4)
U3BOB DS1,2,3,4(A4)
U4COC DS1,2,3,4(A3)
DS1, DS2, DS3, DS4 DL-416
DIG 1 DIG 2 DIG 3 DIG 4 DIG 5 DIG 6 DIG 7 DIG 8 DIG 9 DIG 10 DIG 11 DIG 12 DIG 13 DIG 14 DIG 15 DIG 16
U3AOA
U3AOB
U3AIB
U3AOD
U3AID
U3AOG
U3AIG
SIP'S
R16, 2.2K
R17, 3.3K
R18, 2.2K
R19, 2.2K
R20, 2.2K
R21, 3.3K
R22, 3.3K
R23, 39
R24, 39
R25, 39
R28, 1.5K
NOTE UNLESS OTHERWISE SPECIFIED



REV
FCN
BY
DATE
APP
+5VA
R28
U3C
74LS189
U5C
4016
U4A
CD4514B
+5VC
U5D-5
U5D-3
U8D
CD4093BE
F≈1.6 KHZ
R15
4.99 K
C28
.1/50V
C29
.1 POLY
R13
750
R14
750
Q2
2N3638A
Q3
2N3638A
+5VB
U3BIE
(A4)
U4CIC
(A3)
MV57124 (22 PLCS)
CH1
CH2
CONT
TRIG
GATE
BRST
E.W.
T.I.
50Ω
CMP
ON
MANUAL
LSN
TLK
SRQ
REM
DIG1
DIG2
DIG3
DIG4
DIG5
DIG6
DIG7
DIG8
DIG9
DIG10
DIG11
U4B
ULN
2003A
U6C
ULN
2003A
U9D
ULN
2003A
C27
.1/50V
C30
.1/50V
C31
.1/50V
U3B-15
C24
100/16V
C23
.1
C20
.1
U4C-15
C25
100/16V
C26
.1
TGD
U3B
U4C
ULN2033A
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN
S. CHERMACK
DATE
9-7-79
PROJ ENGR
RELEASE APPROV
R. CONERO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030
DO NOT SCALE DWG
SCALE
WAVETEK
SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC
DISPLAY/LOGIC
MODEL NO
859
DWG NO
0103-00-0690
REV
H
CODE IDENT
23338
SHEET 2 OF 2

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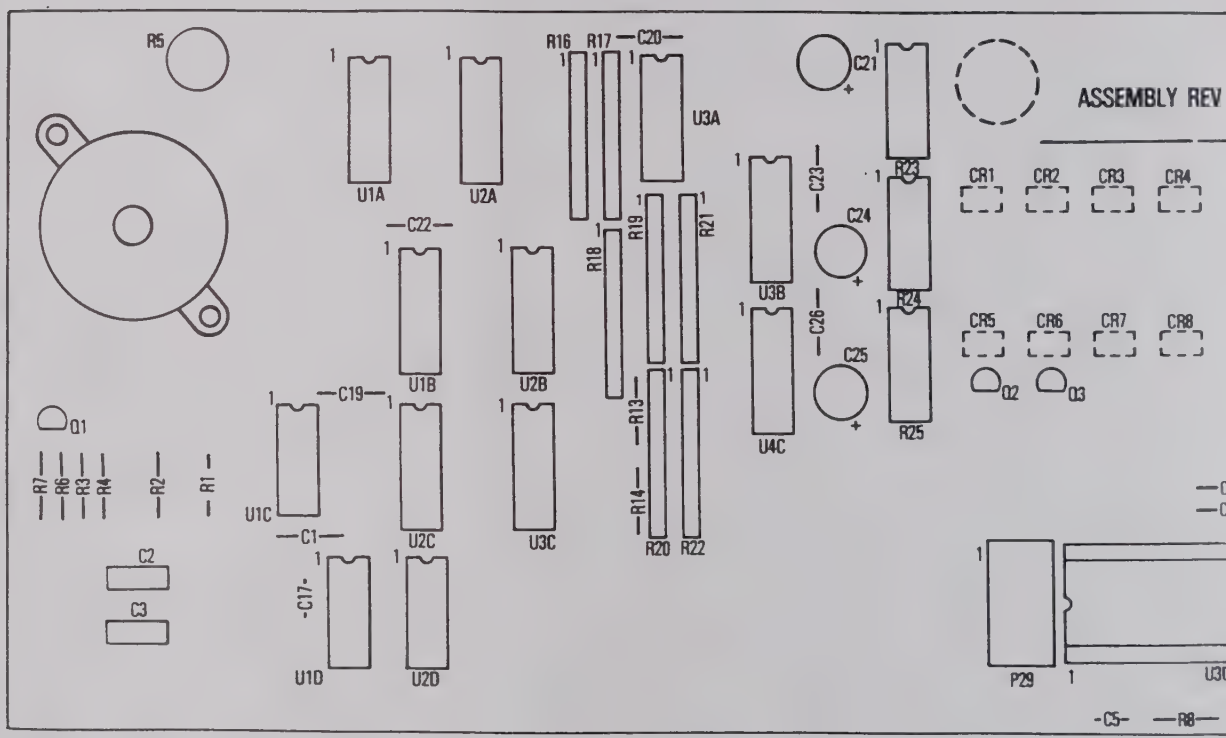

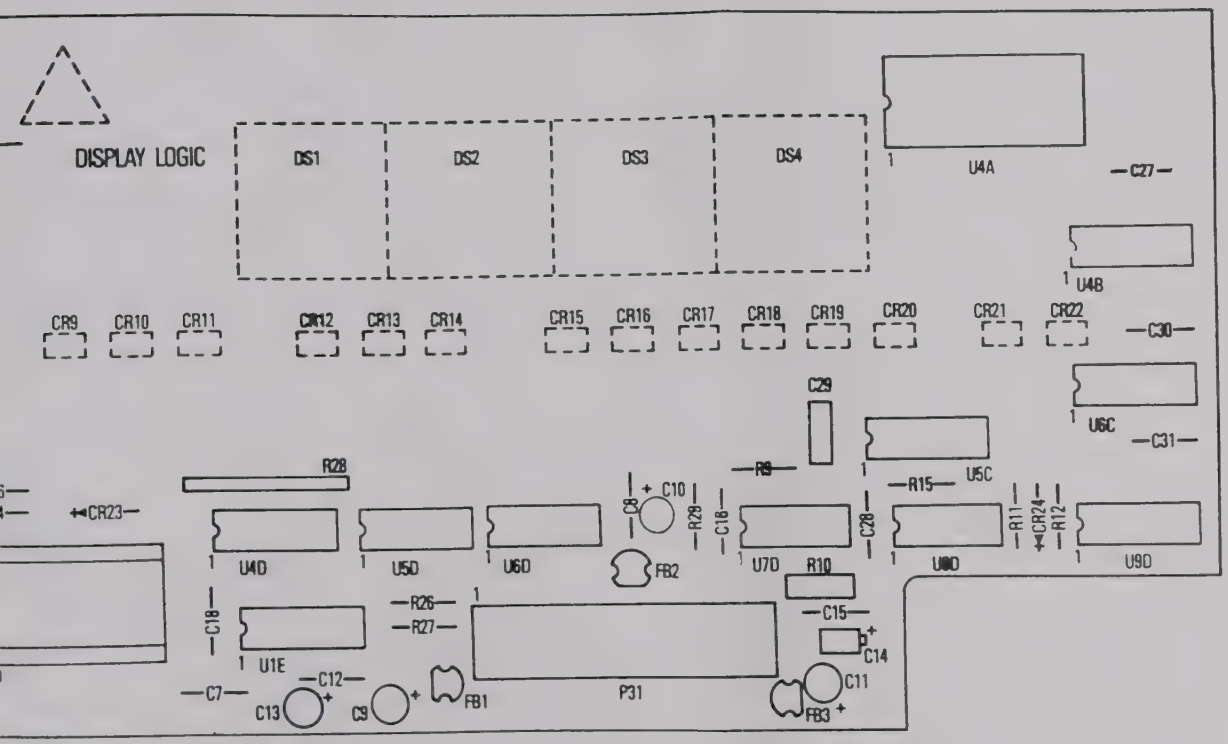

MADE FROM 0100-00-0690-3B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK
MATERIAL	PROJECT		TITLE: DISPLAY LOGIC
	MFG APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES .XX .030		
	DO NOT SCALE DWG		MODEL NO: 859
	SCALE		DWG NO: 1100-00-0690 REV: E
			FSCM NO: 23338 SHEET 1 OF 1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MF
NONE	ASSY DRWG. DISPLAY/ LOGIC	0101-00
NONE	SCHEMATIC. DISPLAY/ LOGIC	0103-00
C1 C12 C16 C18 C19 C20 C22 C23 C26 C27 C28 C30 C31 C4 C6 C7 C8	CAP CER. MON. 1MF. 50V	CAC03Z5
C5	CAP. CER. 47PF. 1KV	DD-470
C15	CAP. MICA. 1000PF. 500V	DM19-10
C17	CAP. MICA. 220PF. 500V	DM15-22
C21 C24 C25	CAP ELECT. 100MF. 25V RADIAL LEAD. SP 20	CRE SER
C2 C29 C3	CAP. MYLAR. 1MF. 100V	225P104
C14	CAP. TANT. 1MF. 35V	150D105
C10 C11 C9	CAP. TANT. 22MF. 15V	196D226
C13	CAP. TANT. 27MF. 35V	196D276
NONE	DISPLAY	859-069
NONE	SKT. IC. 40PIN	DILB-40
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-00

WAVETEK PARTS LIST

TITLE

PCA. DISPLAY/LOGIC

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MF
DS1 DS2	DISPLAY. 18 SEGMENT ALPHANUMERIC	HDSP-65
NONE	BEEPER	KBS-27D
FB1 FB2 FB3	BALUN CORE	2873000
R5	POT. TRIM. 20K	91AR20K
R26 R27 R6 R7 R9	RES. MF. 1/8W. 1%. 1K	RN55D-1
R4 R8	RES. MF. 1/8W. 1%. 100K	RN55D-1
R3	RES. MF. 1/8W. 1%. 130K	RN55D-1
R11	RES. MF. 1/8W. 249K	RN55D-2
R15 R29	RES. MF. 1/8W. 1%. 4 99K	RN55D-4
R1 R2	RES. MF. 1/8W. 1%. 511	RN55D-5
R13 R14	RES. MF. 1/8W. 1%. 750	RN55D-7
R12	RES. MF 1/8W. 1%. 90 9K	RN55D-9
R10	RES. MF. 1/2W. 1%. 1 5M	RN65D-1
R28	RES NETWK	785-1R1
R17 R21 R22	RES MODULE	4310R-1
R16 R18 R19 R20	RES MODULE	4310R-1

WAVETEK PARTS LIST

TITLE

PCA. DISPLAY/LOGIC

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

R-PART-NO	MFGR	WAVETEK NO	QTY/PT
-0690	WVTK	0101-00-0690	1
-0690	WVTK	0103-00-0690	1
V104Z050A	CORNG	1500-01-0405	17
	CRL	1500-04-7011	1
F	ARCO	1500-11-0201	1
J	ARCO	1500-12-2100	1
ES 100/25	CAPAR	1500-31-0102	3
1WD3	SPRAG	1500-41-0444	3
9035A2	SPRAG	1500-71-0502	1
9015KA1	SPRAG	1500-72-2601	3
0035TE4	SPRAG	1500-72-7602	1
	WVTK	1700-00-0690	1
-108	BURND	2100-03-0030	1
	ARTWR	2100-05-0024	4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R23 R24 R25	RES MODULE 39 OHM	3148390	AB	4770-00-0026	3
CR23	DIODE	1N746A	FAIR	4801-01-0746	1
CR24	DIODE	1N4148	FAIR	4807-02-6666	1
CR1 CR10 CR11 CR12 CR13 CR14 CR15 CR16 CR17 CR18 CR19 CR2 CR20 CR21 CR22 CR3 CR4 CR5 CR6 CR7 CR8 CR9	LED	4899-00-0020	WVTK	4899-00-0020	22
Q1 Q2 Q3	TRANS	2N3638A	CARTR	4901-03-6381	3
NONE	CABLE ASSY	CA-D14IDSP-E-CD-005	CA	6002-00-0003	1
NONE	ASSY. RIBBON CABLE	922522-34-02-11	AP	6002-00-0006	1
U4B U6C U9D	IC	ULN2003A	SPRAG	7000-20-0300	3
U3A U3B U4C	IC	ULN2033A	SPRAG	7000-20-3300	3
U4A	IC	CD4514BE	RCA	7000-45-1400	1
U5C	IC	CD40161BE	RCA	7004-01-6100	1
U1E U4D	IC	8T26	SIG	8000-08-2600	2
U1C U8D	IC	CD4093BE	RCA	8000-40-9300	2
U1D	IC	74LS27	TI	8000-74-2710	1
U2D	IC	74LS32	TI	8000-74-3210	1

ASSEMBLY NO.	REV
1100-00-0690	

PAGE 1

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA, DISPLAY/LOGIC	1100-00-0690	

PAGE 3

R-PART-NO	MFGR	WAVETEK NO	QTY/PT
08	HP	2400-03-0011	2
-3A	KYCRA	3000-00-0068	1
902	FARIT	3100-00-0002	3
	BECK	4600-02-0301	1
001F	TRW	4701-03-1001	5
003F	TRW	4701-03-1003	2
503F	TRW	4701-03-1503	1
493F	TRW	4701-03-2493	1
991F	TRW	4701-03-4991	2
110F	TRW	4701-03-5110	2
500F	TRW	4701-03-7500	2
092F	TRW	4701-03-9092	1
504F	TRW	4701-23-1504	1
5K	BECK	4770-00-0010	1
01-332	BOURN	4770-00-0023	3
02-222	BOURN	4770-00-0024	4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U5D U6D	IC	74LS74	TI	8000-74-7410	2
U3D	IC	AY-5-3600PRO	GI	8005-36-0000	1
U7D	IC	74LS132	TI	8007-41-3210	1
U2C	IC	74LS157	TI	8007-41-5710	1
U1A U1B U2A U2B U3C	IC	74LS189	TI	8007-41-8910	5

ASSEMBLY NO.	REV
1100-00-0690	

PAGE 2

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA, DISPLAY/LOGIC	1100-00-0690	

PAGE 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROTECH#	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE

PARTS LIST
PCA, DISPLAY/LOGIC

MODEL NO	DWG NO	REV
859	1100-00-0690	J
CAGE CODE 23338	SHEET 1 OF 1	

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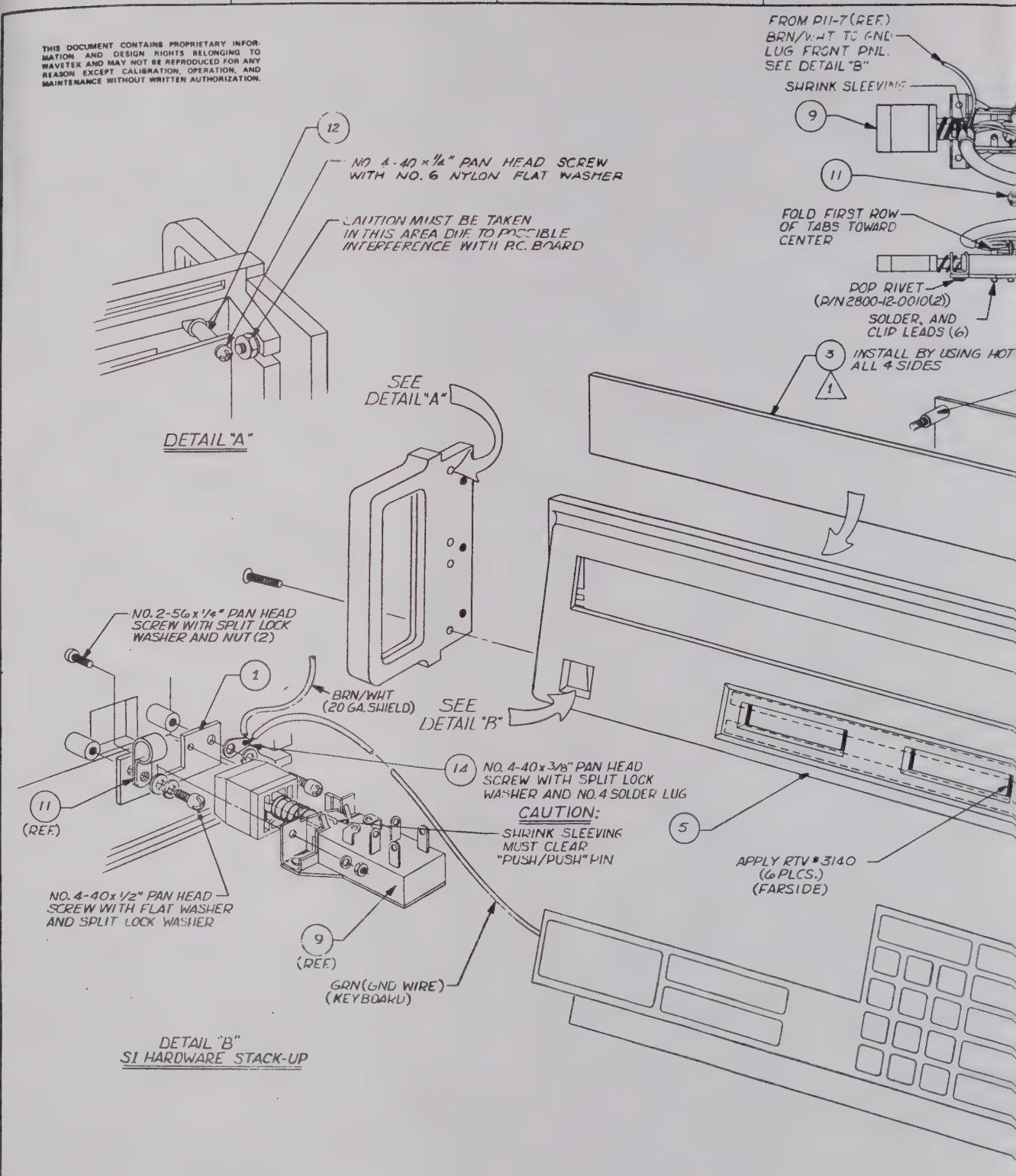
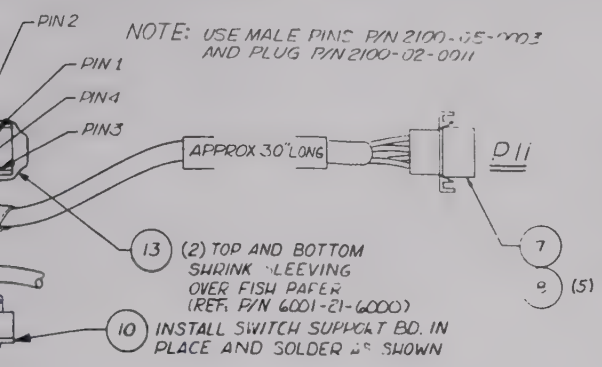


1 LOCATE BY CENTERING IN CUTOUT WITH EQUAL GAP AROUND ALL EDGES.

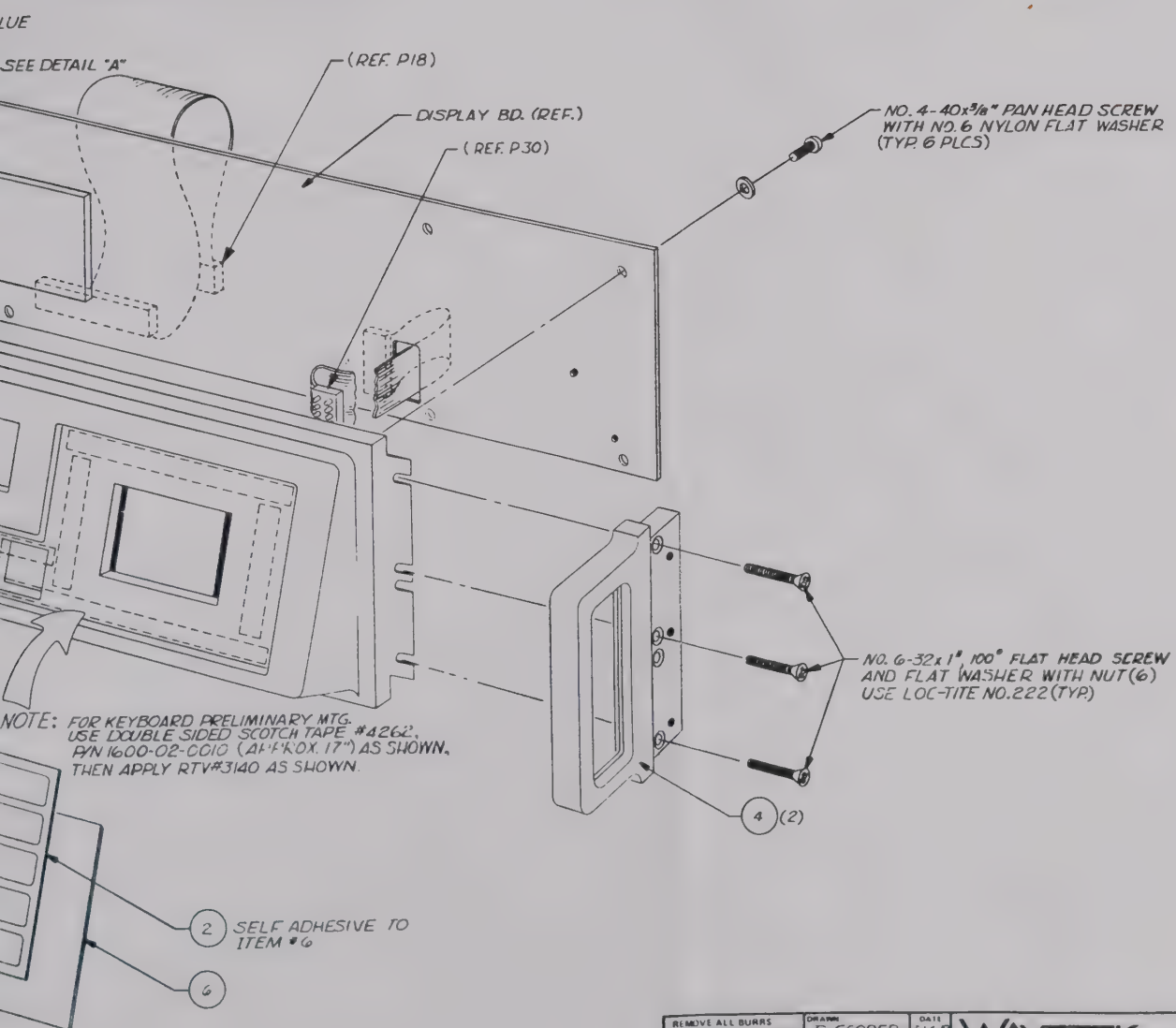
NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
C	FCN [illegible]	[illegible]	7-16-80	[illegible]
-	35 [illegible]	[illegible]	4/16/80	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]



POWER SWITCH (S1) WIRING

P11 WIRE LIST			
PIN NO.	WIRE GA.	COLOR	DESTINATION
1	20	GRN	S1-2
2	20	BLK	S1-3
3	20	RED	S1-1
4		NOT USED	
5		NOT USED	
6	20	WHT	S1-4
7	20	BRN/WHT	SHIELD
8		NOT USED	
9		NOT USED	



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 3-4-80	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY FRONT PANEL (A1)
	RELEASE APPROV V. CONERO 4/2/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1°		
	DO NOT SCALE DWG		MODEL NO 859 · DWG NO 0102-00-0671 · REV C
	SCALE		CODE IDENT 23338 · SHEET 1 OF 1

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FRONT PAN	0102-00-0671	WVTK	0102-00-0671	1
1	BRKT, SWITCH MTG.	172-7703	WVTK	1400-00-7703	1
13	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	2
5	FRONT PANEL, MODIFIED FROM: 1400-00-7031	175-8469	WVTK	1400-00-8469	1
2	KEYBOARD OVERLAY	859-9070	WVTK	1400-00-9070	1
3	PLEX, FRONT PANEL	859-9080	WVTK	1400-00-9080	1
4	HANDLE, WHITE FROM: 1400-00-6951	172-3152	WVTK	1400-01-3152	2
10	SWITCH SUPPORT BD	859-0750	WVTK	1700-00-0750	1
7	PLUG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
14	SOLDER LUG	11A144	ZIER	2100-04-0025	1
8	PIN, MALE	350629-1	AMP	2100-05-0003	5
11	CABLE CLAMP	835	SMITH	2800-00-0010	1
12	STANDOFF, MALE/FEMALE 250H, 250ROUND, 4-40	8200	SMITH	2800-02-0029	1
9	SWITCH, POWER	5102-00-0006	WVTK	5102-00-0006	1
6	KEYBOARD	2SMD200P75079	CRL	5108-00-0003	1

WAVETEK PARTS LIST	TITLE: FRONT PANEL	ASSEMBLY NO.: 1101-00-0671	REV
		PAGE 1	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST FRONT PANEL
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX ±.010 ANGLES ±1; XX ±.030		
	DO NOT SCALE DWG		MODEL NO: 859 / DWG NO: 1101-00-0671 / REV: D
	SCALE		CODE IDENT NO: 23338 / SHEET 1 OF 1

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BISHOP GRAPHICS, ACCUPRESS
REORDER NO. A-3864

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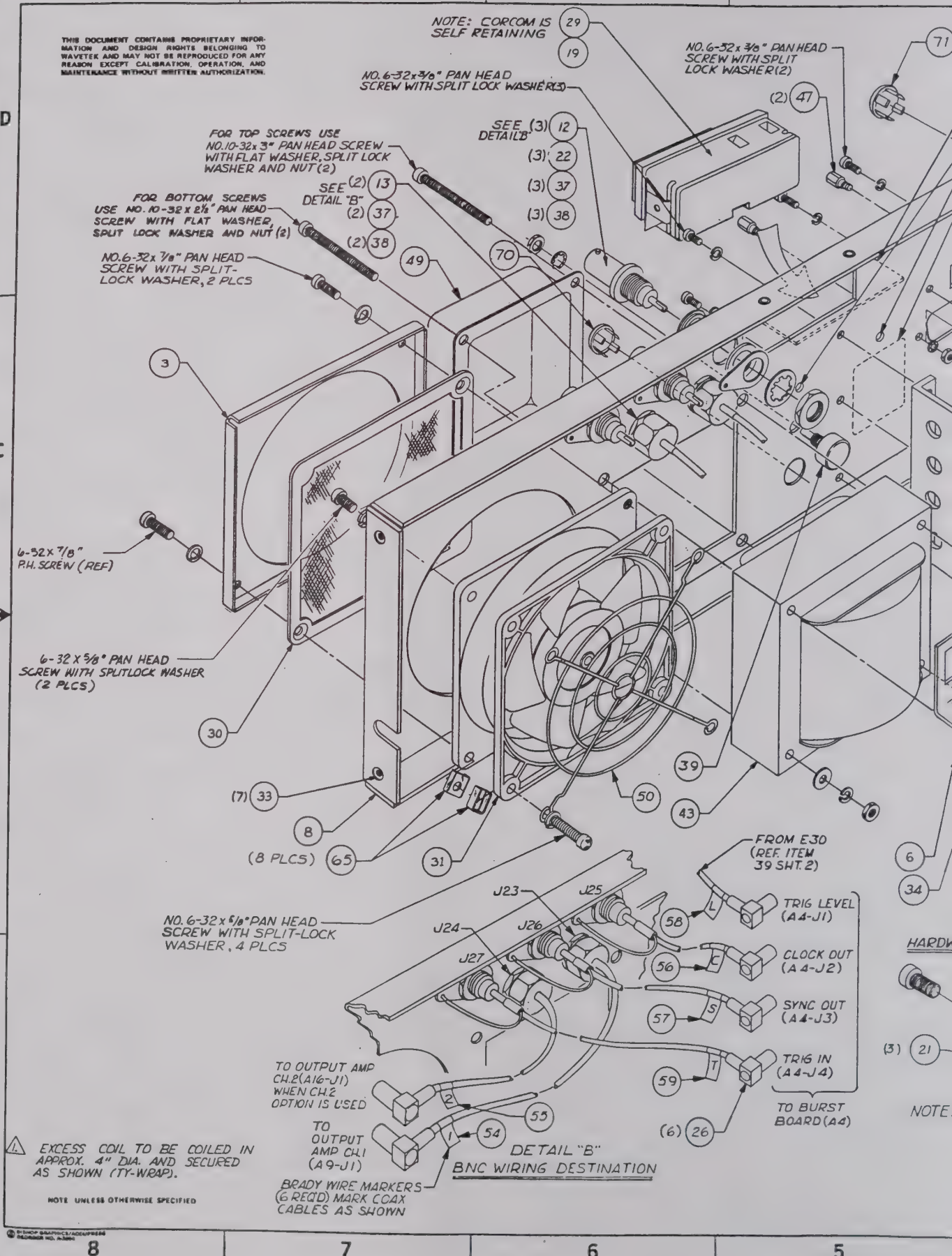
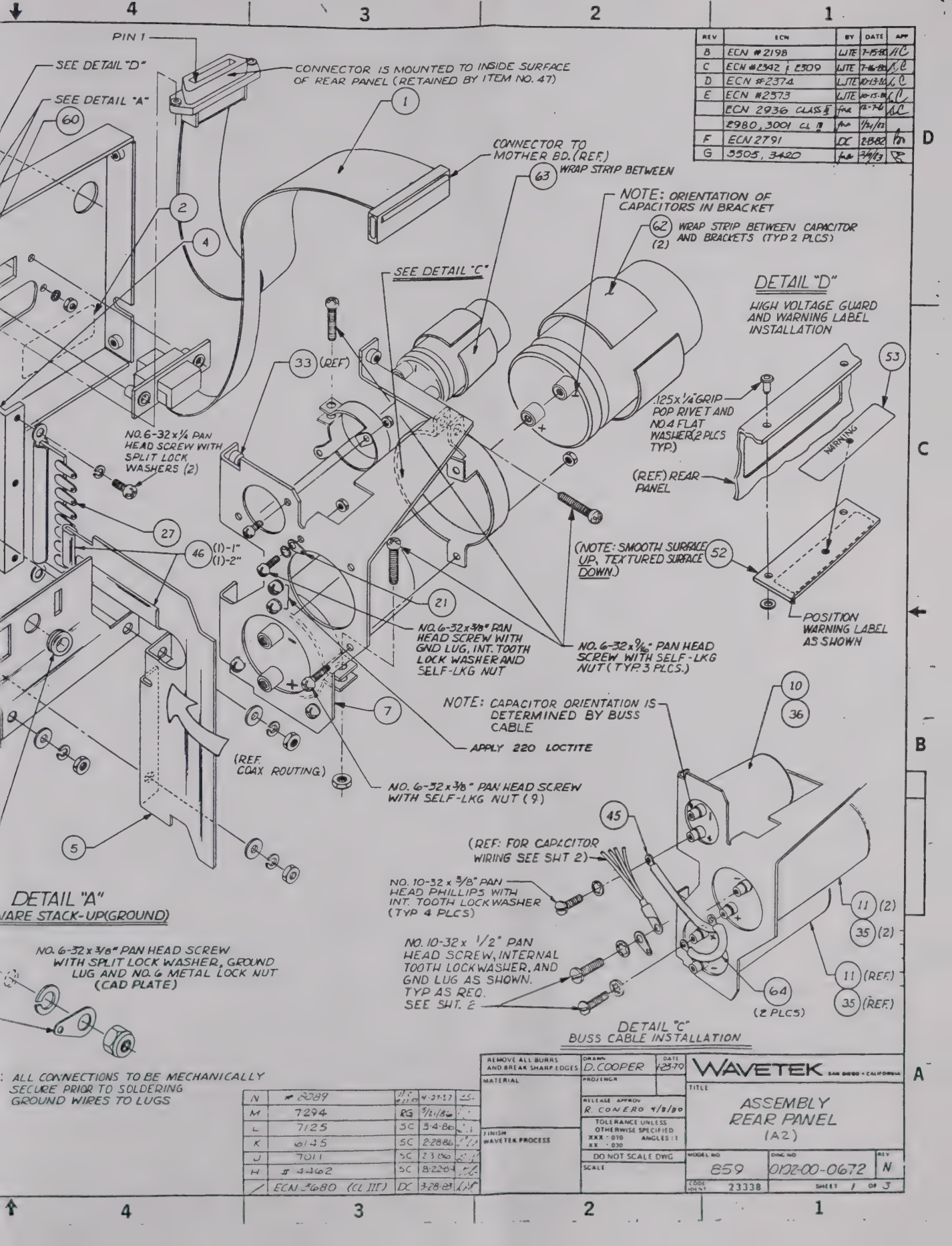


⚠ EXCESS COIL TO BE COILED IN APPROX. 4" DIA. AND SECURED AS SHOWN (TY-WRAP).

NOTE UNLESS OTHERWISE SPECIFIED



REV	ECN	BY	DATE	APP
B	ECN #2198	WJTE	7-15-80	
C	ECN #2342 & 2309	WJTE	7-16-80	
D	ECN #2374	WJTE	10-13-80	
E	ECN #2373	WJTE	10-15-80	
	ECN 2936 CLASS II		12-7-6	
	2980, 3001 CL III		1/21/82	
F	ECN 2791	DC	2-18-82	
G	3505, 3420		2/9/83	

N	# 8089		4-27-87	
M	7294	RG	5/21/86	
L	7125	SC	3-4-86	
K	6145	SC	2-28-86	
J	7011	SC	2-3-86	
H	# 4462	SC	8-22-84	
/	ECN 3680 (CL III)	DC	3-28-83	

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN D. COOPER DATE 4-23-79

PROJENGR

RELEASE APPROV R. CONERO 4/8/80

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE ASSEMBLY REAR PANEL (A2)

MODEL NO 859 DWG NO 0102-00-0672 REV N

CODE IDENT 23338 SHEET 1 OF 3

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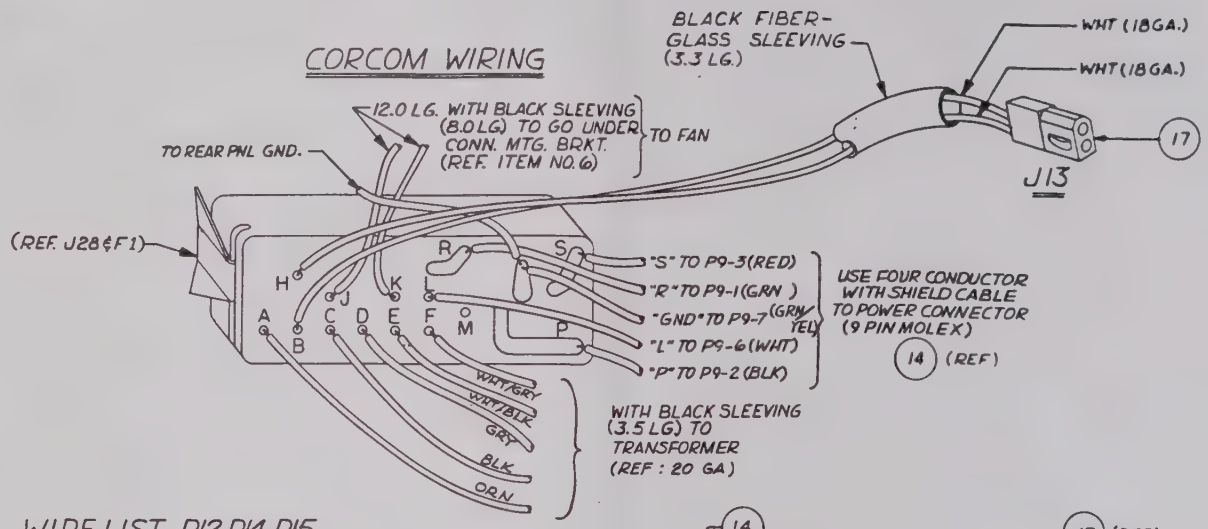
CORCOM WIRING



WIRE LIST P12, P14, P15

P12

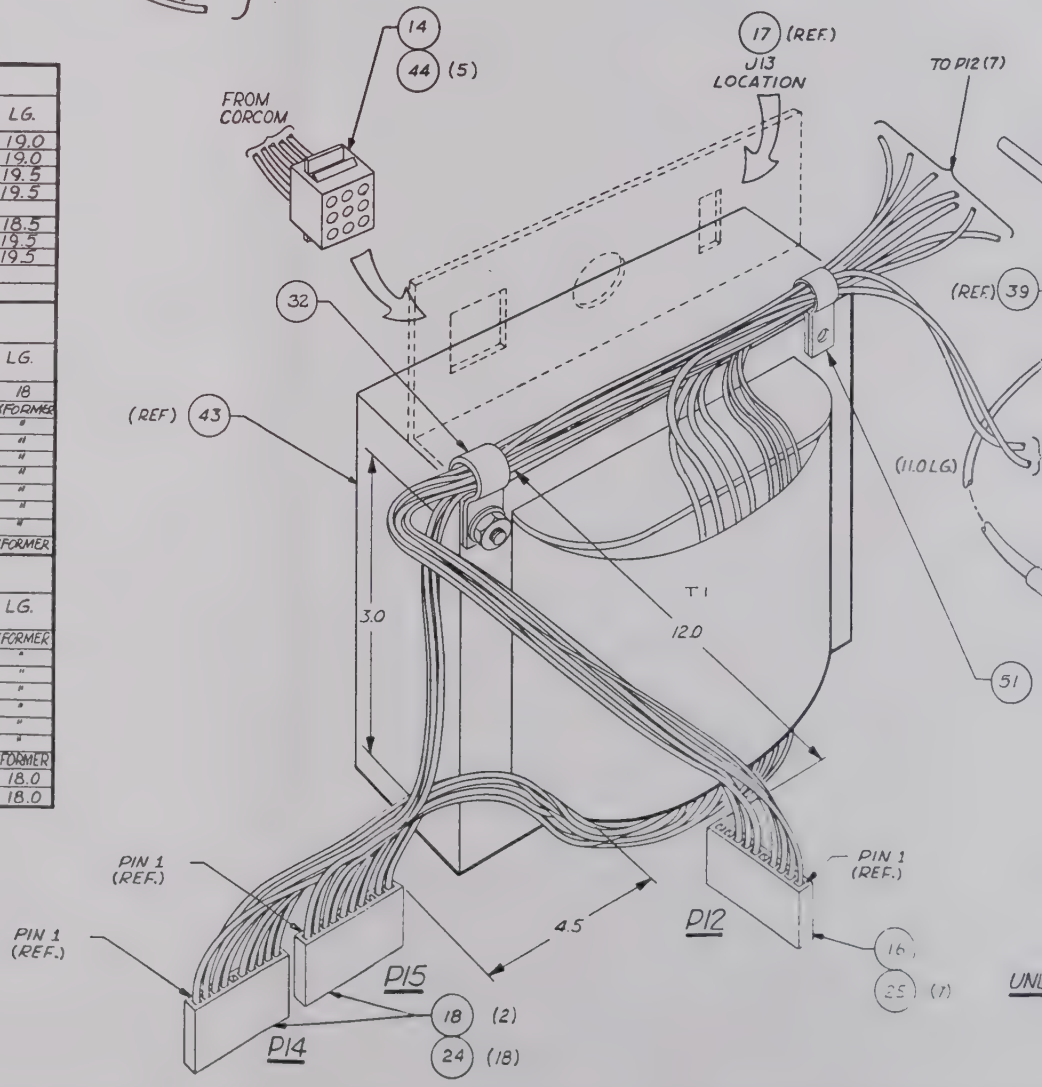
PIN NO.	WIRE GA.	COLOR	FROM	LG.
1	18	WHT	DIGITAL GND.	19.0
2	18	WHT	DIGITAL GND.	19.0
3	18	RED	+5V UNREG.	19.5
4	18	RED	+5V UNREG.	19.5
5			N.C.	
6	18	BLU	-2V UNREG.	18.5
7	18	GRN	-5.2V UNREG.	19.5
8	18	GRN	-5.2V UNREG.	19.5
9			N.C.	
10			N.C.	

P14

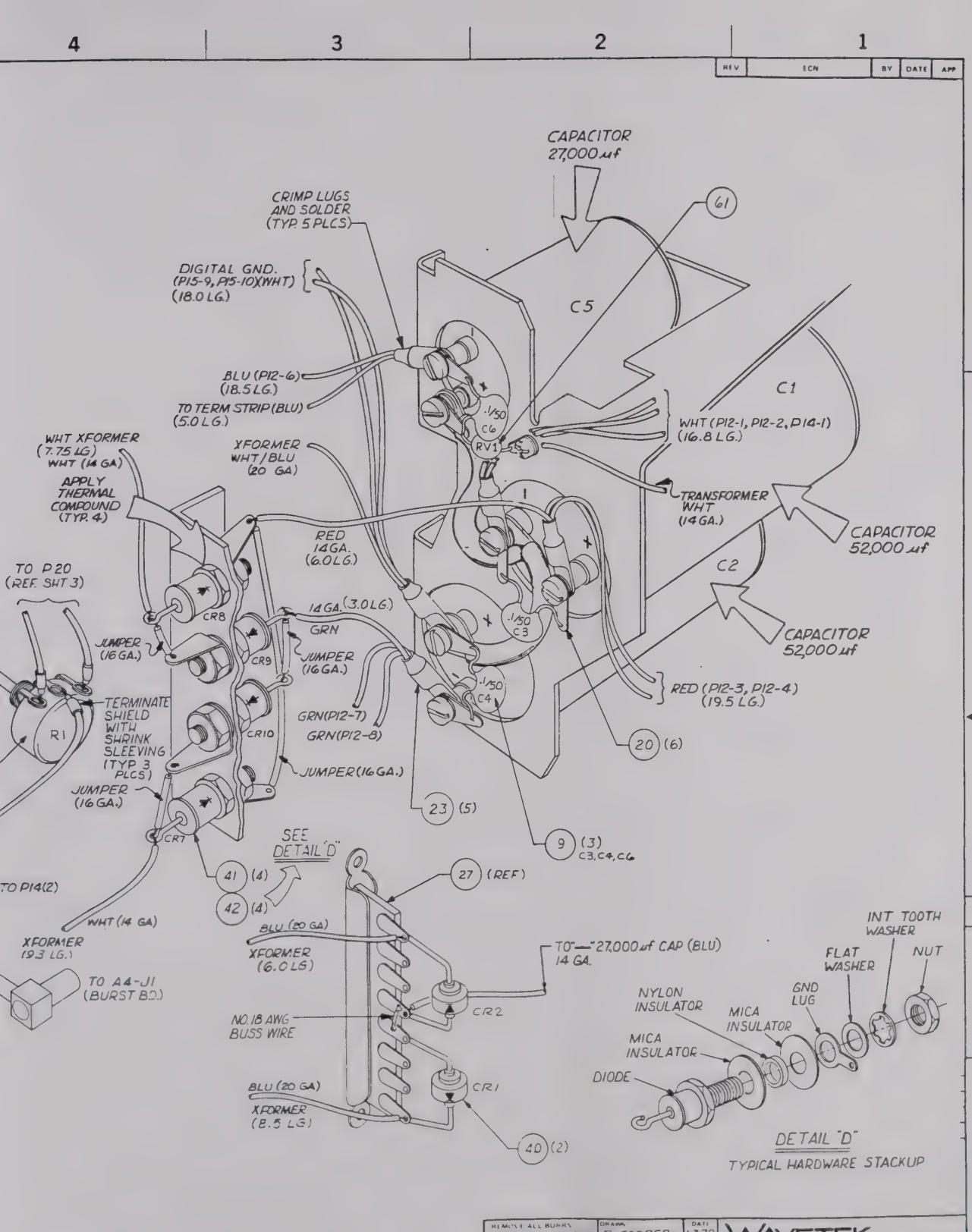
PIN NO.	WIRE GA.	COLOR	FROM	LG.
1	18	WHT	DIGITAL GND.1	18
2	24	RED	UNR+15/1	XFORMER
3	24	WHT/RED	F15-RT/1	"
4	24	RED	UNR-15/1	"
5			N.C.	"
6	24	BRN	UNR+15/2	"
7	24	BRN	UNR-15/2	"
8	24	WHT/BRN	F10-RT/2	"
9	20	YEL	UNR+30H/2	"
10	20	YEL	UNR+30L/2	XFORMER

P15

PIN NO.	WIRE GA.	COLOR	FROM	LG.
1	20	WHT	UNR+30H/1	XFORMER
2	20	WHT	UNR+30L/1	"
3	22	WHT/VIO	UNR-15O5H	"
4	22	WHT/VIO	UNR-15O5L	"
5	24	WHT/GRN	UNR±15CT	"
6	24	GRN	UNR+15	"
7	24	GRN	UNR-15	"
8			SHIELD	XFORMER
9	18	WHT	DIGITAL GND.	18.0
10	18	WHT	DIGITAL GND.	18.0



NOTE UNLESS OTHERWISE SPECIFIED



ALL WIRES TO BE 18GA.
UNLESS OTHERWISE SPECIFIED.

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 1-3-79	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROTENGR		TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV R. GONERO 4/8/80		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG.	MODEL NO 859	DWG NO 0102-00-0672 REV M
	SCALE	CODE IDENT NO 23338	SHEET 2 OF 3

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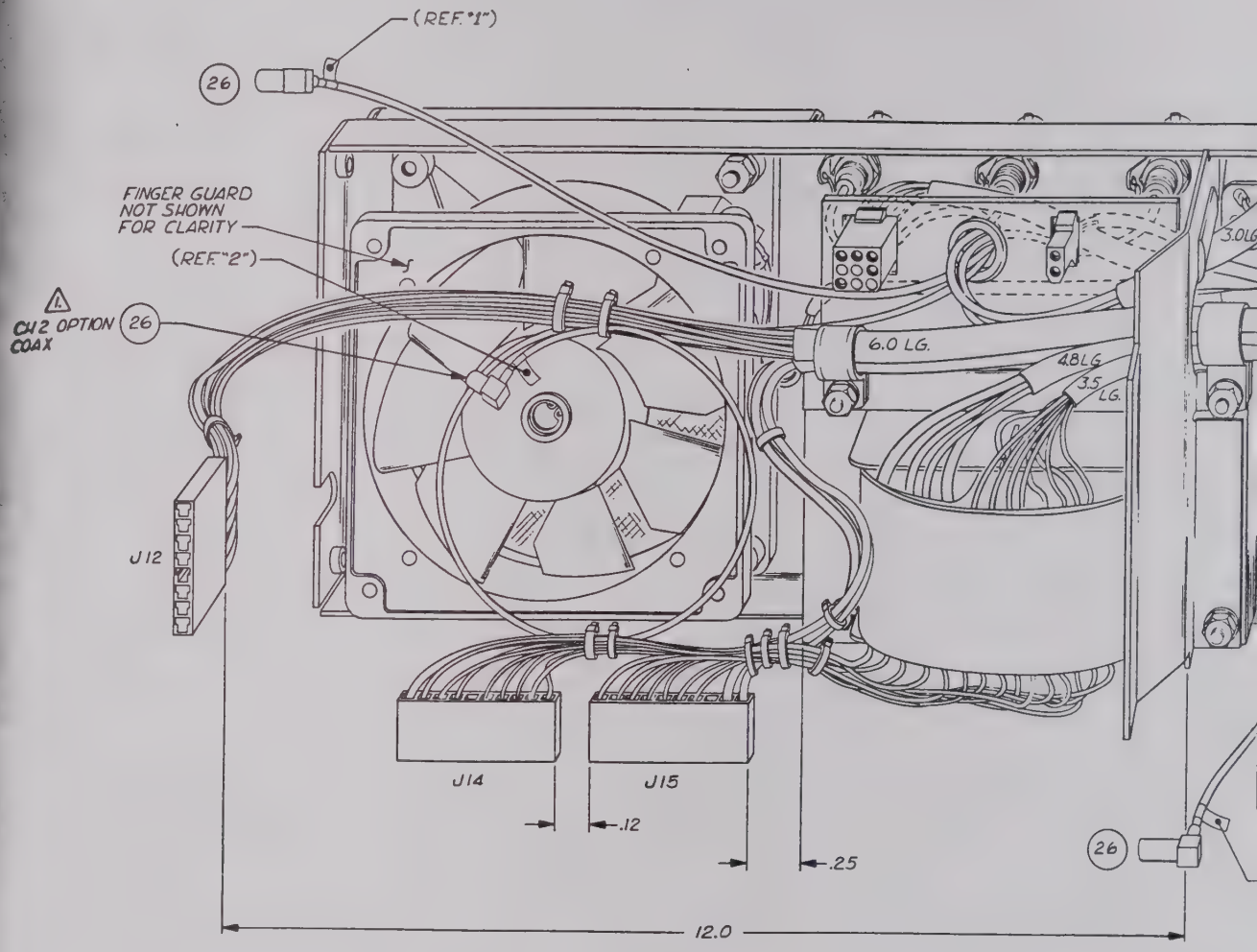
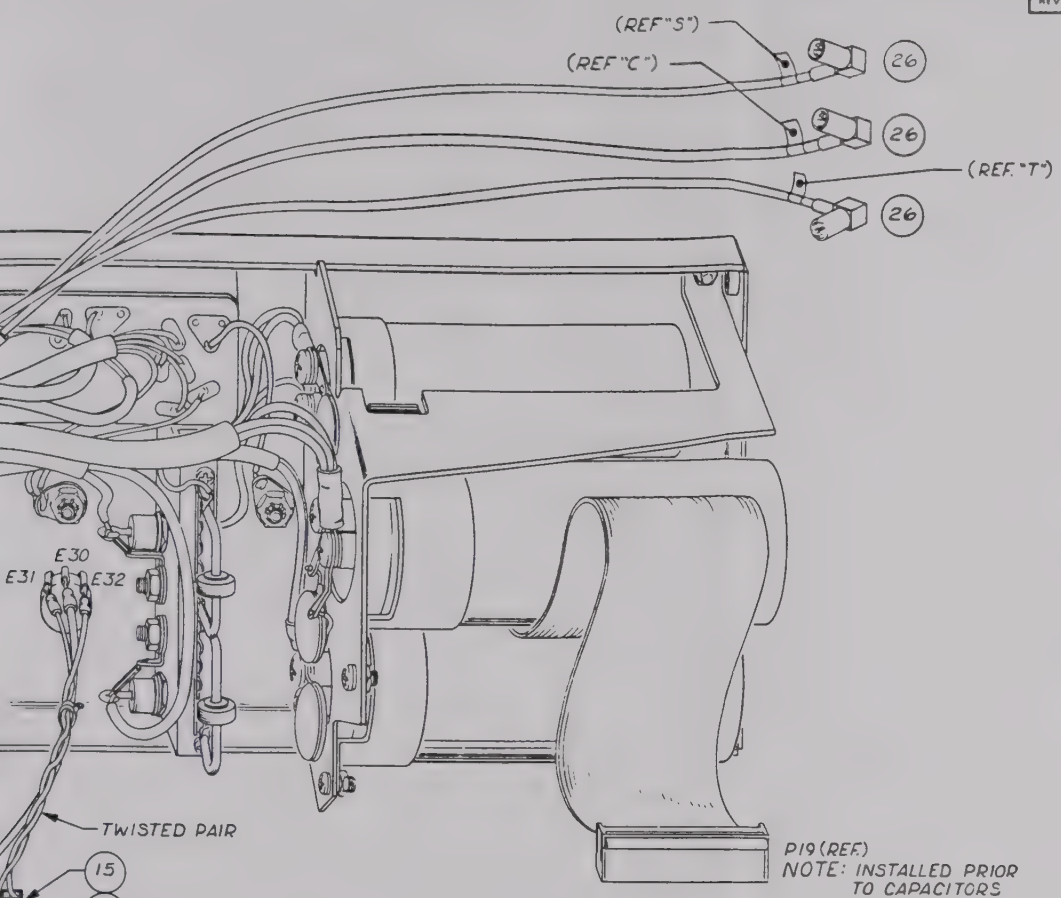


3. COLOR OF PIGTAIL OF COAXES SHOULD REFLECT THEIR LENGTH (PER WAVETEK STANDARDS ASSEMBLY MANUAL.)
2. ALL WIRE LENGTHS ARE APPROX.
⚠ INSTALL TY-WRAPS AS SHOWN

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP



P20

PIN NO.	WIRE COLOR	TO	GA.	LENGTH
1	WHT/RED	E32	22	9"
2	PIN INSTALLED FOR GRIP ONLY			
3	WHT/BRN	E31	22	9"

(REF "L")

REAR PANEL BNC CONNECTORS

P/L ITEM NO	FROM	TO	WIRE	LG.	FUNCTION	WKR
26	J23	A9-J1	RG174 U	16"	CH1 OUTPUT	1
26	J24	A16-J1	RG174/U	16"	CH2 OUTPUT	2
26	J25	A4-J2	RG174/U	33"	CLOCK OUT	C
26	J26	A4-J3	RG174/U	62"	SYNC OUT	S
26	J27	A4-J4	RG174/U	14"	TRIG IN	T
26	E30	A4-J1	RG174/U	8"	TRIG LEVEL	L

⚠1

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 9-28-73	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY REAR PANEL
FINISH WAVETEK PROCESS	RELEASE APPROV R. CONERO 9/8/80		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES 1 XX ± .030		
	DO NOT SCALE DWG.	MODEL NO 259	DWG NO 0102-00-0672 REV IVi
	SCALE	CODE IDENT 23338	SHEET 3 OF 3

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART NO	MFGR	WAVETEK NO	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-0672	WVTK	0102-00-0672	1
NONE	TRANSFORMER	859-0023	WVTK	1204-00-0023	1
45	ASSY, BUSS CABLE 859-0672	859-2746	WVTK	1207-00-2746	1
1	PCA, OPIB ADDRESS	859-0730	WVTK	1208-00-0730	1
3	SCREEN COVER	172-7523	WVTK	1400-00-7523	1
60	LABEL, OPTION	172-8880	WVTK	1400-00-8880	1
4	BRACKET, POWER DIODE	859-9253	WVTK	1400-00-9253	1
5	STOP, AIR	859-9263	WVTK	1400-00-9263	1
6	BRACKET, CONN MTG	859-9273	WVTK	1400-00-9273	1
7	BRACKET	859-9283	WVTK	1400-00-9283	1
8	REAR PANEL	859-9290	WVTK	1400-00-9290	1
49	END BELL	859-0574	WVTK	1400-01-0574	1
52	GUARD, HIGH VOLTAGE	859-1391	WVTK	1400-01-1391	1
53	LABEL, CAUTION	859-1400	WVTK	1400-01-1400	1
62	POLYESTER FILM REF: 1600-99-0002	175-3191	WVTK	1400-01-3191	2
63	REF: 1600-99-0002	859-4791	WVTK	1400-01-4791	1

WAVETEK PARTS LIST | TITLE: REAR PANEL | ASSEMBLY NO. 1101-00-0672 | REV U

REFERENCE DESIGNATORS	PART DESCRIPTION	C
24	PIN	0
25	CONN PINS	8
26	CONN	2
27	TERMINAL STRIP	3
29	FUSE, 3A, 250V, S-B	3
31	FAN REF: 2600-99-0002	1
30	FAN FILTER	5
50	FINGER GUARD	6
NONE	CABLE CLAMP	E
32	CABLE CLAMP	7
51	CABLE CLAMP	8
33	INSERT # 6	7
65	MOUNTING CLIP	5
34	GROMMET, RUBBER	2
35	CAP, MTG, BKT	F
36	CAP, MTG, BKT	FH

WAVETEK PARTS LIST | TITLE: REAR PANEL

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	POLYESTER FILMSHIELD				
9	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	3
10	CAP, ELEC, 27000MF, 10V	FAHM27000-10-A2	CDE	1500-32-7301	1
11	CAP, ELEC, 52000MF, 15V	FAHM52000-15-B3	CDE	1500-35-2301	2
12	BNC CONN	UG657/U	AMPH	2100-01-0003	3
13	BNC CONN	KC-19-152	KING	2100-01-0006	2
14	PLUG, 9PIN	03-06-2091	MOLEX	2100-02-0011	1
16	CONN HOUSING	1-87025-6	AMP	2100-02-0077	1
17	CONN RECEPTACLE	03-06-1022	MOLEX	2100-02-0083	1
18	CONN HOUSING	09-50-7101	MOLEX	2100-02-0087	2
15	HEADER, CONN 3 PIN	640440-3	AMP	2100-02-0117	1
19	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
20	TERM, LOCK LUG	1414-10	SMITH	2100-04-0007	6
21	TERM, LOCK LUG	1414-6	SMITH	2100-04-0009	3
22	SOLDER LUG	1497	SMITH	2100-04-0012	3
23	LUG	35	ILSCO	2100-04-0018	5
44	PIN, FEMALE	350628-1	AMP	2100-05-0002	5

WAVETEK PARTS LIST | TITLE: REAR PANEL | ASSEMBLY NO. 1101-00-0672 | REV U

REFERENCE DESIGNATORS	PART DESCRIPTION	OR
NONE	RIVET, ALUM 1/8X1/4L .126-.187	112
37	WASHER, SHOULDER	266
38	NYLON FLAT WASHER	226
70	PLUG BUTTON	264
71	PLUG BUTTON	266
46	RUBBER SEAL	447
54	WIRE MARKER "1"	TMM
55	WIRE MARKER "2"	TMM
56	WIRE MARKER "C"	TMM
57	WIRE MARKER "S"	TMM
58	WIRE MARKER "L"	TMM
59	WIRE MARKER "T"	TMM
47	JACKSOCKET ASSY. OPIB BUSS	609
39	5K POT LOCK ADJ	MA2
61	VARISTOR	489
40	DIODE	MR7

WAVETEK PARTS LIST | TITLE: REAR PANEL

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-1884

REV	ECN	BY	DATE	APP

IO-MFGR-PART-NO	MFGR	WAVETEK NO	QTY
-50-0105	MOLEX	2100-05-0025	18
027-3	AMP	2100-05-0047	7
-843	AMPH	2100-07-0009	6
98	SMITH	2100-09-0014	1
1.003	LITFU	2400-05-0024	1
PXR-2282	ETNI	2600-00-0005	1
2	PAMOT	2600-01-0005	1
175	IMC	2600-01-0007	1
	RICH	2800-00-0009	1
-1503	CONCD	2800-00-0010	1
	SMITH	2800-00-0016	1
11-106-13	SOTCO	2800-09-0017	7
011	IMC	2800-09-0033	8
7	SMITH	2800-10-0005	1
R	STM	2800-12-0006	2
R-2	STM	2800-12-0007	1

	ASSEMBLY NO.	REV
	1101-00-0672	U
	PAGE 3	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	DIODE, POWER RECT. SCHOTTKY, STUD MOUNT, 30A	30FQ030	IR	4806-00-0018	4
42	DIODE, MOUNTING KIT REF: 4899-00-0018	40-8021	IR	4899-00-0019	4
64	SHRINK TUBING, 3/8 IN	FIT-221-3/8	ALPHA	6001-20-6000	3

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	REAR PANEL	1101-00-0672	U
		PAGE 5	

-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
-0408	AVDEL	2800-12-0043	2
	SMITH	2800-27-0004	5
-N-385	AMTOM	2800-28-0005	5
/DP-500 BLACK	HEYCO	2800-35-0003	1
(BLACK)	HEYCO	2800-35-0004	1
	ACCUR	3000-00-0005	2
1	BRADY	3000-00-0076	1
2	BRADY	3000-00-0077	1
C	BRADY	3000-00-0078	1
S	BRADY	3000-00-0079	1
-	BRADY	3000-00-0080	1
T	BRADY	3000-00-0081	1
325	T&B	3000-00-0154	1
040S502UC	A-B	4600-05-0209	1
-00-0045	HVTK	4799-00-0048	1
	MOT	4801-02-0751	2

	ASSEMBLY NO.	REV
	1101-00-0672	U
	PAGE 4	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE
	RELEASE APPROV		PARTS LIST REAR PANEL
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 1101-00-0672 U
	SCALE	CUSTOMER 23338	SHEET 1 OF 1

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J41
1	SO1
2	N.C.
3	SO2

TO J2 ON REAR PANEL (A2)

J40
1	TIMER(M1)
2	DG3
3	N.C.

TO M1 ON REAR PANEL (A2)

J42
PTRVL (J1B-76) →
TO J1 ON BURST BD (A4)

R11 2.15M

J14
1	DIG GND1
2	UNR+15/1
3	F15-RT/1
4	UNR-15/1
5	
6	UNR+15/2
7	UNR-15/2
8	F15-RT/2
9	UNR+30H/2
10	UNR+30L/2

J20
1	+15V
2	NC
3	-15V

J15
1	UNR+35H/1
2	UNR+35L/1
3	UNR-ISO5H
4	UNR-ISO5L
5	UNR±15CT
6	UNR+15
7	UNR-15
8	SHIELD
9	DIG GND2
10	DIG GND3

FROM REAR PANEL

FROM HI CURRENT POWER SUPPLY BOARD

J16
1	DG2
2	-2V SEN
3	-5.2V SEN
4	+5V SEN
5	-2V
6	-5.2V
7	-5.2V
8	+5V
9	+5V
10	AG

J17
1	DG2
2	-2V SEN
3	-5V SEN
4	+15V IN
5	-2V
6	-5.2V
7	-5.2V
8	+5V
9	+5V
10	-15V IN

UNR +15/1 — C1 .01 — F15-RT/1 — C2 .01 — UNR-15/1

UNR +15/2 — C3 .01 — F15-RT/2 — C4 .01 — UNR-15/2

UNR +30H/2 — C5 .01 — UNR+30L/2 — UNR+30H/1 — C6 .01 — UNR+30L/1

UNR-ISO 5H — C7 .01 — UNR-ISO 5L — UNR+15 — C8 .01 — UNR±15CT — C9 .01 — UNR-15

TDLY

ODLY

TRF

TIBRF

FOR [illegible] USE ONLY

(A10) LO AMP P.S.
A	J10	B
UNR+15	50	UNR+15
UNR-15	49	UNR-15
AG	48	AG
UNR±15CT	47	UNR±15CT
+15SEN	46	+15SEN
+15V(.5A)	45	+15V(.5A)
15V(.5A)	44	15V(.5A)
	43	
-15SEN	42	-15SEN
	41	
UNR-ISO5H	40	UNR-ISO5L
UNR-ISO5L	39	UNR-ISO5L
UNR-ISO5H	38	UNR-ISO5H
UNR-ISO5H	37	UNR-ISO5H
	36	
ISO+5	35	ISO+5
ISO+5	34	ISO+5
ISOCOM	33	ISOCOM
ISOCOM	32	ISOCOM
	31	
35SEN/1	30	35SEN/1
F35H/1	29	F35H/1
F35L/1	28	F35L/1
	27	
UNR-ISO5H	26	UNR+35L/1
UNR+35H/1	25	UNR+35H/1
	24	
35SEN/2	23	35SEN/2
F35H/2	22	F35H/2
F35L/2	21	F35L/2
	20	
UNR+35L/2	19	UNR+35L/2
UNR+35H/2	18	UNR+35H/2
	17	
	16	
F+15/2	15	F+15/2
	14	
F-15/2	13	F-15/2
	12	
F15-RT/2	11	F15-RT/2
UNR-15/2	10	UNR-15/2
UNR+15/2	9	UNR+15/2
	8	
F+15/1	7	F+15/1
	6	
F-15/1	5	F-15/1
	4	
UNR-15/1	3	UNR-15/1
F15-RT/1	2	F15-RT/1
UNR+15/1	1	UNR+15/1

(A9) CHANNEL 2 OUTPUT AMP
A	J9	B
-15V	50	-15V
CH1/CH2	49	CH1/CH2
AG	48	AG
AG	47	AG
	46	
+15V	45	+15V
	44	
-2V	43	-2V
	42	
-5.2V	41	-5.2V
-5.2V	40	-5.2V
	39	
+5V	38	+5V
+5V	37	+5V
	36	
DG2	35	DG2
	34	
F-15/2	33	F-15/2
	32	
F15-RT/2	31	F15-RT/2
F35L/2	30	F35L/2
	29	
F+15/2	28	F+15/2
	27	
F35H/2	26	F35H/2
	25	
	24	
DG2	23	DG2
	22	
DG2	21	DG2
DG2	20	WRF2
DG2	19	DG2
CH1/CH2 ID	18	C10
CI2	17	AD0
CI3	16	AD1
CI4	15	AD2
CI5	14	AD3
CI6	13	AD4
CI7	12	AD5
COB/MNTG	11	AD6
CO1/EXE	10	AD7
CO2/BEEP	9	S
CO3	8	AA0
CO4	7	AA1
CO5	6	AA2
CO6	5	AA3
CO7	4	STRB1
STRB1	3	AA4
AA6	2	AA5
	1	

(A9) CHANNEL 1 OUTPUT AMP
A	J8	B
-15V	50	-15V
CH1/CH2	49	CH1/CH2
AG	48	AG
AG	47	AG
	46	
+15V	45	+15V
	44	
-2V	43	-2V
	42	
-5.2V	41	-5.2V
-5.2V	40	-5.2V
	39	
+5V	38	+5V
+5V	37	+5V
	36	
DG2	35	DG2
	34	
F-15/1	33	F-15/1
	32	
F15-RT/1	31	F15-RT/1
F35L/1	30	F35L/1
	29	
F+15/1	28	F+15/1
	27	
F35H/1	26	F35H/1
	25	
	24	
DG2	23	DG2
	22	
DG2	21	DG2
DG2	20	WRF1
DG2	19	DG2
	18	C10
CI2	17	AD0
CI3	16	AD1
CI4	15	AD2
CI5	14	AD3
CI6	13	AD4
CI7	12	AD5
COB/MNTG	11	AD6
CO1/EXE	10	AD7
CO2/BEEP	9	S
CO3	8	AA0
CO4	7	AA1
CO5	6	AA2
CO6	5	AA3
CO7	4	STRB1
STRB2	3	AA4
AA6	2	AA5
	1	

(A7) CLOCK OSCILLATOR
A	J7	B
-15V	50	-15V
	49	
AG	48	AG
AG	47	AG
	46	
+15V	45	+15V
	44	
-2V	43	-2V
	42	
-5.2V	41	-5.2V
-5.2V	40	-5.2V
	39	
+5V	38	+5V
+5V	37	+5V
	36	
DG2	35	DG2
DG2	34	DG2
DG2	33	DG2
DG2	32	DG2
DG2	31	DG2
DG2	30	DG2
DG2	29	GATE
DG2	28	DG2
DG2	27	GATE/
DG2	26	DG2
DG2	25	OBUR
DG2	24	DG2
DG2	23	DG2
	22	
DG2	21	DG2
	20	
DG2	19	DG2
	18	C10
CI2	17	AD0
CI3	16	AD1
CI4	15	AD2
CI5	14	AD3
CI6	13	AD4
CI7	12	AD5
COB/MNTG	11	AD6
CO1/EXE	10	AD7
CO2/BEEP	9	S
CO3	8	AA0
CO4	7	AA1
CO5	6	AA2
CO6	5	AA3
CO7	4	STRB1
STRB2	3	AA4
AA6	2	AA5
	1	

(A4) BURS
A	J6
-15V	50
	49
AG	48
AG	47
	46
+15V	45
	44
-2V	43
	42
-5.2V	41
-5.2V	40
	39
+5V	38
+5V	37
	36
DG2	35
DG2	34
DG2	33
DG2	32
	31
DG2	30
GATE	29
DG2	28
GATE/	27
DG	26
OBUR	25
DG2	24
DG2	23
	22
DG2	21
	20
DG2	19
	18
CI2	17
CI3	16
CI4	15
CI5	14
CI6	13
CI7	12
COB/MNTG	11
CO1/EXE	10
CO2/BEEP	9
CO3	8
CO4	7
CO5	6
CO6	5
CO7	4
STRB1	3
AA6	2
	1

+5V — R5-1.5K
2 —
3 —
14 — A BUS 1/
15 — A BUS 3/
16 — A BUS 5/
17 — A BUS 7/
18 — A BUS 9/
19 — A BUS 11/
10 — A BUS 13/

+5V — R6-1.5K
12 — A BUS 0/
13 — A BUS 2/
14 — A BUS 4/
15 — A BUS 6/
16 — A BUS 8/
17 — A BUS 10/
18 — A BUS 12/
19 — A BUS 14/
10 —

+5V — R7-1.5K
2 — MRST
3 — BOP REQ
14 — MRST/
15 —
16 —
17 — BWRP
18 — BR/W
19 — BM/IO
10 — BOP REQ/

+5V — R8-1.5K
12 — D BUS 4/
13 — D BUS 2/
14 — RDK BD1
15 — D BUS 7/
16 — D BUS 5/
17 — D BUS 3/
18 — BWRPS
19 — D BUS 1/
10 — D BUS 0/

+5V — R9
— D BUS 6/
— DISPEN/

1. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSY REF DES A12.

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
B	1507	LDU	5-15-81	RPC
C	ECN 84G1	RO	8-84	

P35 HI — R1 78.7Ω — TDLY CH2
P33 HI — R2 78.7Ω — ODLY CH2
P34 HI — R3 78.7Ω — TRF CH2
P35 HI — R4 78.7Ω — TIBRF CH2

+5V — C12 1000UF 35V — DG2
C10 .01, C11 .01
-2V

CHANNEL 1 (A8) DELAY/WIDTH

A	J5	B
-15V	50	-15V
	49	
AG	48	AG
AG	47	AG
	46	
+15V	45	+15V
	44	
-2V	43	-2V
	42	
-5.2V	41	-5.2V
-5.2V	40	-5.2V
	39	
+5V	38	+5V
+5V	37	+5V
	36	
DG2	35	DG2
DG2	34	DG2
DG2	33	DG2
DG2	32	DG2
	31	DG2
TIBRF	30	
	29	DG2
TRF	28	
	27	DG2
ODLY	26	
	25	DG2
TDLY	24	
DG2	23	DG2
	22	
DG2	21	DG2
WRF1	20	DG2
DG2	19	DG2
	18	CI0
CI2	17	AD0
CI3	16	AD1
CI4	15	AD2
CI5	14	AD3
CI6	13	AD4
CI7	12	AD5
COI/MNTG	11	AD6
COI/EXE	10	AD7
CO2/BEEP	9	S
CO3	8	AA0
CO4	7	AA1
CO5	6	AA2
CO6	5	AA3
CO7	4	STRB1
STRB2	3	AA4
AA6	2	AA5
	1	

CHANNEL 2 (A8) DELAY/WIDTH

A	J4	B
-15V	50	-15V
	49	
AG	48	AG
AG	47	AG
	46	
+15V	45	+15V
	44	
-2V	43	-2V
	42	
-5.2V	41	-5.2V
-5.2V	40	-5.2V
	39	
+5V	38	+5V
+5V	37	+5V
	36	
DG2	35	DG2
DG2	34	DG2
DG2	33	DG2
DG2	32	DG2
	31	DG2
TIBRF	30	
	29	DG2
TRF	28	
	27	DG2
ODLY	26	
	25	DG2
TDLY	24	
DG2	23	DG2
	22	
DG2	21	DG2
WRF2	20	CG2
DG2	19	DG2
CH1/CH2CTD	18	CI0
CI2	17	AD2
CI3	16	AD1
CI4	15	AD2
CI5	14	AD3
CI6	13	AD4
CI7	12	AD5
COI/MNTG	11	AD6
COI/EXE	10	AD7
CO2/BEEP	9	S
CO3	8	AA0
CO4	7	AA1
CO5	6	AA2
CO6	5	AA3
CO7	4	STRB2
STRB1	3	AA4
AA6	2	AA5
	1	

J18

1	DBUS0/1	18	-15V
2	DBUS1/	19	+5V
3	DBUS2/	20	DG1
4	DBUS3/	21	+5V
5	DBUS4/	22	DG1
6	DBUS5/	23	+5V
7	DBUS6/	24	+5V
8	DBUS7/	25	ABUS0/
9	ABUS1/	26	DG1
10	ABUS2/	27	+5V
11	ABUS3/	28	RDKY BD1
12	ABUS4/	29	BWRPS
13	ABUS5/	30	DG1
14	ABUS6/	31	DG1
15	DG1	32	DG1
16	+5V	33	CO2/BEEP
17	-15V	34	DISPEN/

DISPLAY CONNECTOR TOP VIEW

A J3 B

DG3	100	DG3
DG3	99	DG3
	98	
ABUS17	97	ABUS0/
ABUS3/	96	ABUS2/
ABUS5/	95	ABUS4/
ABUS7/	94	ABUS6/
ABUS9/	93	ABUS8/
ABUS11/	92	ABUS10/
ABUS13/	91	ABUS12/
	90	ABUS14/
	89	
ADI2/	88	EOI
DAV	87	IFC
ATN	86	ADI4/
ADI3/	85	ADI1/
ADI0/	84	REN
NRFD	83	NDAC
SRQ	82	DIO4
DIO5	81	DIO6
DIO1	80	DIO7
DIO3	79	DIO2
ISO+5	78	DIO8
ISOCOM	77	ISOCOM
	76	
	75	
	74	
	73	
	72	
	71	
	70	
	69	
	68	
MRST/	67	MRST
	66	
	65	
ISO+5	64	ISO+5
ISO+5	63	ISO+5
ISOCOM	62	ISOCOM
ISOCOM	61	ISOCOM
	60	
	59	
-15V	58	-15V
	57	
	56	
	55	
+15V	54	+15V
-5.2V	53	-5.2V
+5VTL	52	+5VTL
+5VTL	51	+5VTL

A RAM B

+5VTL	50	+5VTL
+5VTL	49	+5VTL
	48	
CI0	47	CI1/CH2ID
AD0	46	CI2
AD1	45	CI3
AD2	44	CI4
AD3	43	CI5
AD4	42	CI6
AD5	41	CI7
AD6	40	COI/MNTG
AD7	39	COI/EXE
S	38	CO2/BEEP
AA0	37	CO3
AA1	36	CO4
AA2	35	CO5
AA3	34	CO6
STRB1	33	CO7
AA4	32	STRB2
AA5	31	AA6
	30	
SYSCLK0	29	SYSCLK1
SYSCLK2	28	SYSCLK3
SYSCLK4	27	SYSCLK5
	26	
	25	
	24	
	23	
DISPEN/	22	RDKY BD1
	21	
	20	
EWRPS	19	BOFREQ
	18	
	17	
PRUN/WAIT	16	MRST1
GENSEL	15	BTAG/
BINTACK	14	VNTREQ1
PDMA0/	13	
BWRP	12	BR1/W
BYNE	11	BWIZO
BOFREQ	10	ACK-C/
	9	
DBUS7	8	DBUS6/
DBUS5/	7	DBUS4/
DBUS3/	6	DBUS2/
DBUS1/	5	DBUS0/
+15	4	+15
	3	
DG3	2	DG3
	1	

A PROC B

+5VTL	50	+5VTL
+5VTL	49	+5VTL
	48	
CI0	47	CI1/CH2ID
AD0	46	CI2
AD1	45	CI3
AD2	44	CI4
AD3	43	CI5
AD4	42	CI6
AD5	41	CI7
AD6	40	COI/MNTG
AD7	39	COI/EXE
S	38	CO2/BEEP
AA0	37	CO3
AA1	36	CO4
AA2	35	CO5
AA3	34	CO6
STRB1	33	CO7
AA4	32	STRB2
AA5	31	AA6
	30	
SYSCLK0	29	SYSCLK1
SYSCLK2	28	SYSCLK3
SYSCLK4	27	SYSCLK5
	26	
	25	
	24	
	23	
DISPEN/	22	RDKY BD1
	21	
	20	
EWRPS	19	BOFREQ
	18	
	17	
PRUN/WAIT	16	MRST1
GENSEL	15	BTAG/
BINTACK	14	VNTREQ1
PDMA0/	13	
BWRP	12	BR1/W
BYNE	11	BWIZO
BOFREQ	10	ACK-C/
	9	
DBUS7	8	DBUS6/
DBUS5/	7	DBUS4/
DBUS3/	6	DBUS2/
DBUS1/	5	DBUS0/
+15	4	+15
+5	3	+15
DG3	2	DG3
	1	

A J2 B

DG3	100	DG3
DG3	99	DG3
	98	
ABUS17	97	ABUS0/
ABUS3/	96	ABUS2/
ABUS5/	95	ABUS4/
ABUS7/	94	ABUS6/
ABUS9/	93	ABUS8/
ABUS11/	92	ABUS10/
ABUS13/	91	ABUS12/
	90	ABUS14/
	89	
ADI2/	88	EOI
DAV	87	IFC
ATN	86	ADI4/
ADI3/	85	ADI1/
ADI0/	84	REN
NRFD	83	NDAC
SRQ	82	DIO4
DIO5	81	DIO6
DIO1	80	DIO7
DIO3	79	DIO2
ISO+5	78	DIO8
ISOCOM	77	ISOCOM
	76	
	75	
	74	
	73	
	72	
	71	
	70	
	69	
	68	
MRST/	67	MRST
	66	
	65	
ISO+5	64	ISO+5
ISO+5	63	ISO+5
ISOCOM	62	ISOCOM
ISOCOM	61	ISOCOM
	60	
	59	
-15V	58	-15V
	57	
	56	
	55	
+15V	54	+15V
-5.2V	53	-5.2V
+5VTL	52	+5VTL
+5VTL	51	+5VTL

A J1 B

DG3	100	DG3
DG3	99	DG3
	98	
ABUS17	97	ABUS0/
ABUS3/	96	ABUS2/
ABUS5/	95	ABUS4/
ABUS7/	94	ABUS6/
ABUS9/	93	ABUS8/
ABUS11/	92	ABUS10/
ABUS13/	91	ABUS12/
	90	ABUS14/
	89	
ADI2/	88	EOI
DAV	87	IFC
ATN	86	ADI4/
ADI3/	85	ADI1/
ADI0/	84	REN
NRFD	83	NDAC
SRQ	82	DIO4
DIO5	81	DIO6
DIO1	80	DIO7
DIO3	79	DIO2
ISO+5	78	DIO8
ISOCOM	77	ISOCOM
	76	PTRVI
TIBRF	75	DG3
	74	
	73	
SOT	72	
	71	
	70	
	69	
	68	
MRST/	67	MRST
	66	
	65	
ISO+5	64	ISO+5
ISO+5	63	ISO+5
ISOCOM	62	ISOCOM
ISOCOM	61	ISOCOM
	60	
	59	
-15V	58	-15V
	57	
CH1OUT	56	CH2OUT
	55	
+15V	54	+15V
-5.2V	53	-5.2V
+5VTL	52	+5VTL
+5VTL	51	+5VTL

A GPIB B

+5VTL	50	+5VTL
+5VTL	49	+5VTL
	48	
CI0	47	CI1/CH2ID
AD0	46	CI2
AD1	45	CI3
AD2	44	CI4
AD3	43	CI5
AD4	42	CI6
AD5	41	CI7
AD6	40	COI/MNTG
AD7	39	COI/EXE
S	38	CO2/BEEP
AA0	37	CO3
AA1	36	CO4
AA2	35	CO5
AA3	34	CO6
STRB1	33	CO7
AA4	32	STRB2
AA5	31	AA6
	30	
SYSCLK0	29	SYSCLK1
SYSCLK2	28	SYSCLK3
SYSCLK4	27	SYSCLK5
	26	
	25	
	24	
	23	
DISPEN/	22	RDKY BD1
	21	
	20	
EWRPS	19	BOFREQ
	18	
	17	
PRUN/WAIT	16	MRST1
GENSEL	15	BTAG/
BINTACK	14	VNTREQ1
PDMA0/	13	
BWRP	12	BR1/W
BYNE	11	BWIZO
BOFREQ	10	ACK-C/
	9	
DBUS7	8	DBUS6/
DBUS5/	7	DBUS4/
DBUS3/	6	DBUS2/
DBUS1/	5	DBUS0/
+15	4	+15
	3	
	2	
	1	

(TOP VIEW) GPIB RIBBON

J19 GPIB

1	DIO1	13	NRFD
2	DIO5	14	150 COM
3	CIFC	15	NDAC
4	DIO6	16	150 COM
5	WEN3	17	IFC
6	DIO7	18	150 COM
7	DIO4	19	SRQ
8	DIO8	20	150 COM
9	EOI	21	ATN
10	REN	22	150 COM
11	DAV	23	SHIELD
12	150 COM	24	150 COM
		25	150 COM
		26	150 COM
		27	150 COM
		28	150 COM
		29	150 COM
		30	ADI4/
		31	150 COM
		32	ADI3/
		33	150 COM
		34	ADI2/
		35	150 COM
		36	ADI1/
		37	150 COM
		38	ADI0/
		39	
		40	

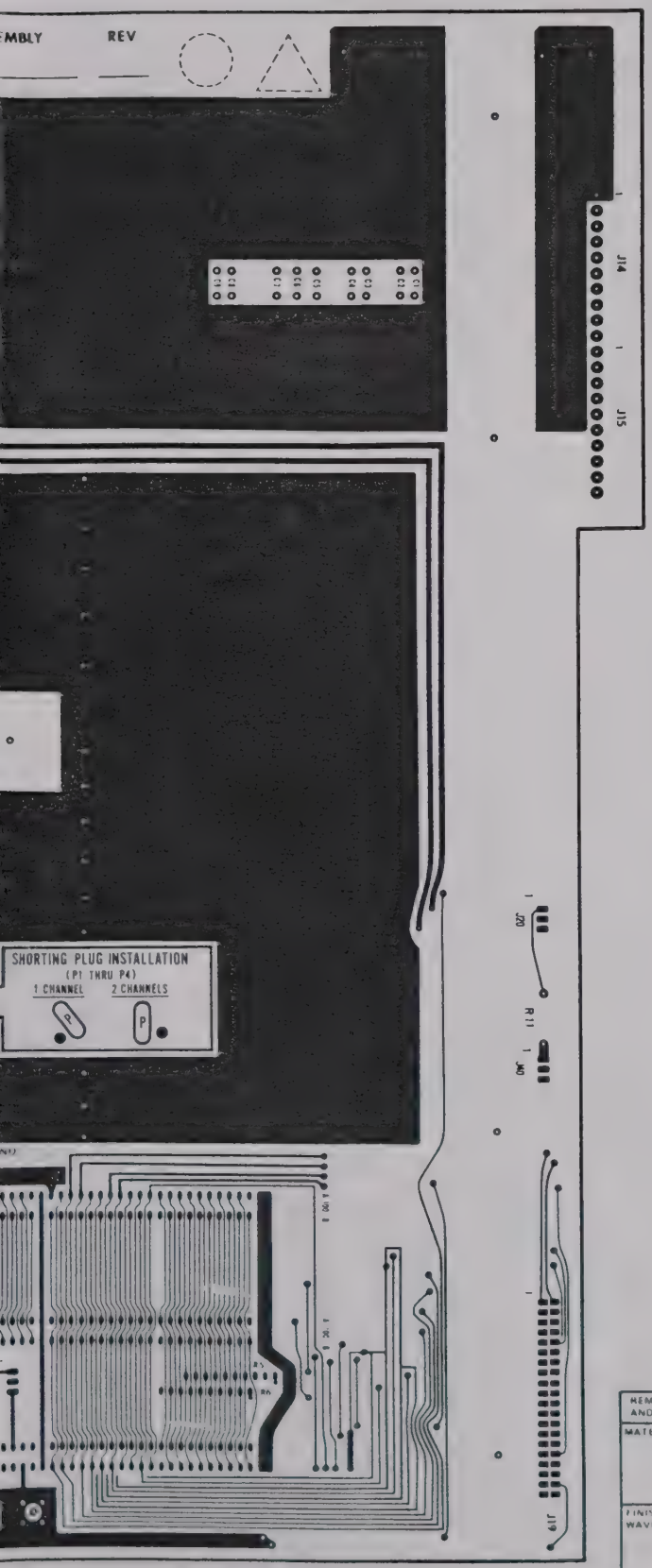
R. CONERO 4/8/80

SCHEMATIC — MOTHER BOARD (A12)

DWG NO 0103-00-0702 REV C

23338 SHEET 1 OF 1

0100-00-0702-2F
0/D1700-00-0702
WAVETEK
MOTHER BOARD
J10
J9
J8
J7
J6
J5
J4
J3
J2
J1
J18
C12
DIG GND



MADE FROM 0100-00-0702-2F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR		TITLE: MOTHER BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES 1 .XX .030		
	DO NOT SCALE DWG	MODEL NO 959	DWG NO 1100-00-0702 REV F
	SCALE		

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NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASBY DRWG, MOTHER	0101-00-0702	WVTK	0101-00-0702	1
NONE	SCHEMATIC, MOTHER	0103-00-0702	WVTK	0103-00-0702	1
C1 C10 C11 C2 C3 C4 C5 C6 C7 C8 C9	CAP, CER, MN, .01MF, 50V	GE50-103ZA	MURAT	1500-01-0310	11
C12	CAP, ELECT, 1000MF, 35V	39D1080035GL6	SPRAG	1500-31-0212	1
NONE	MOTHER	859-0702	WVTK	1700-00-0702	1
J14 J15 J16 J17	CONN HEADER	09-60-1101	MOLEX	2100-02-0088	4
J20 J40 J41	CONN HEADER 3 PIN	640456-3	AMP	2100-02-0116	3
J10 J1A J1B J2A J2B J3A J3B J4 J5 J6 J7 J8 J9	CONN, EDGE CARD-GP	TP1-501-504	TEKA	2100-03-0053	13
J19	HEADER	929836-02-20	A/P	2100-05-0048	1
J18	HEADER	929836-02-17	A/P	2100-05-0049	1
J42	CONN	27-848	AMPH	2100-07-0011	1
NONE	WASHER, NYLON	2676	SMITH	2800-26-0003	2
P32 P33 P34 P35	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	4
NONE	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	12
R10 R9	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	2
R11	RES, MF, 1/8W, 1%, 2.15M	RN55D2154F	TRW	4701-03-2154	1

WAVETEK PARTS LIST	TITLE: PCA, MOTHER	ASSEMBLY NO.: 1100-00-0702	REV
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R1 R2 R3 R4	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	4
R5 R6 R7 R8	RES NETWK	785-1R1.5K	BECK	4770-00-0010	4

WAVETEK PARTS LIST	TITLE: PCA, MOTHER	ASSEMBLY NO.: 1100-00-0702	REV
		PAGE 2	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, MOTHER BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO: 859	DWG NO: 1100-00-0702 REV: C
	SCALE	CODE IDENT: 23338	SHEET 1 OF 1

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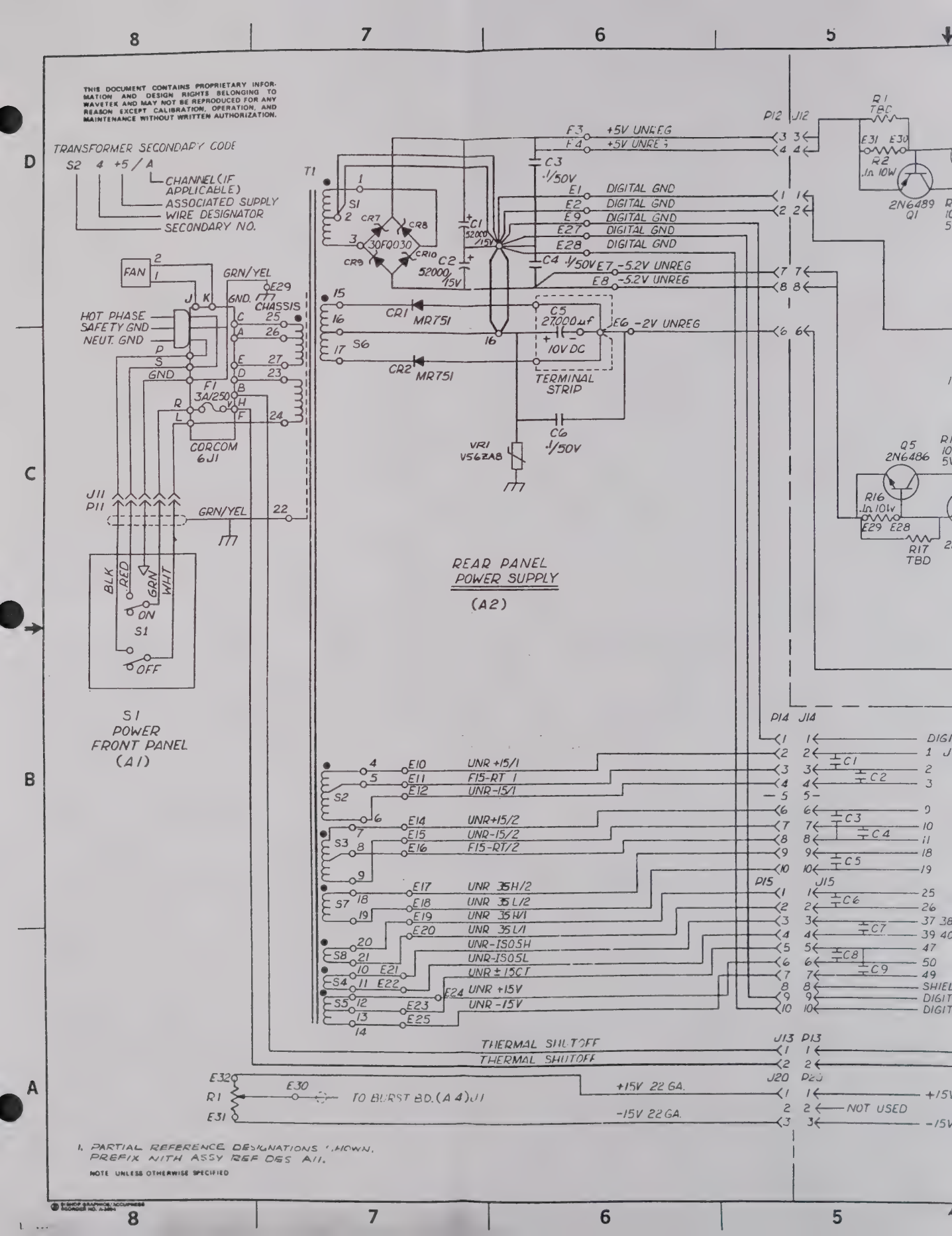
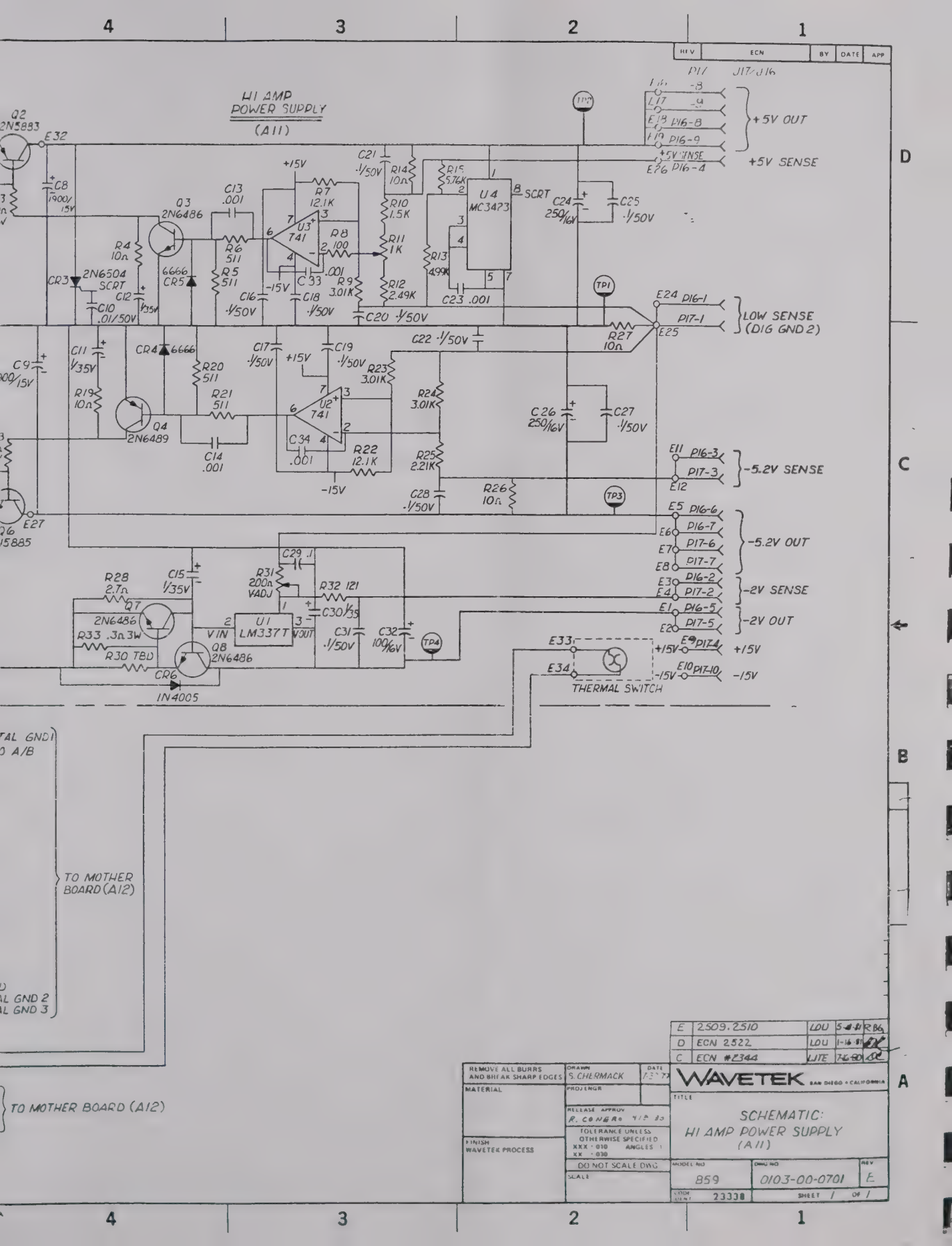


1. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX WITH ASSY REF DES A11.

NOTE UNLESS OTHERWISE SPECIFIED


HI AMP POWER SUPPLY (A11)
+5V OUT
+5V SENSE
LOW SENSE (DIG GND 2)
-5.2V SENSE
-5.2V OUT
-2V SENSE
-2V OUT
+15V
-15V
THERMAL SWITCH
TO MOTHER BOARD (A12)
TO MOTHER BOARD (A12)
WAVETEK
SCHEMATIC: HI AMP POWER SUPPLY (A11)
859
0103-00-0701
E
23338

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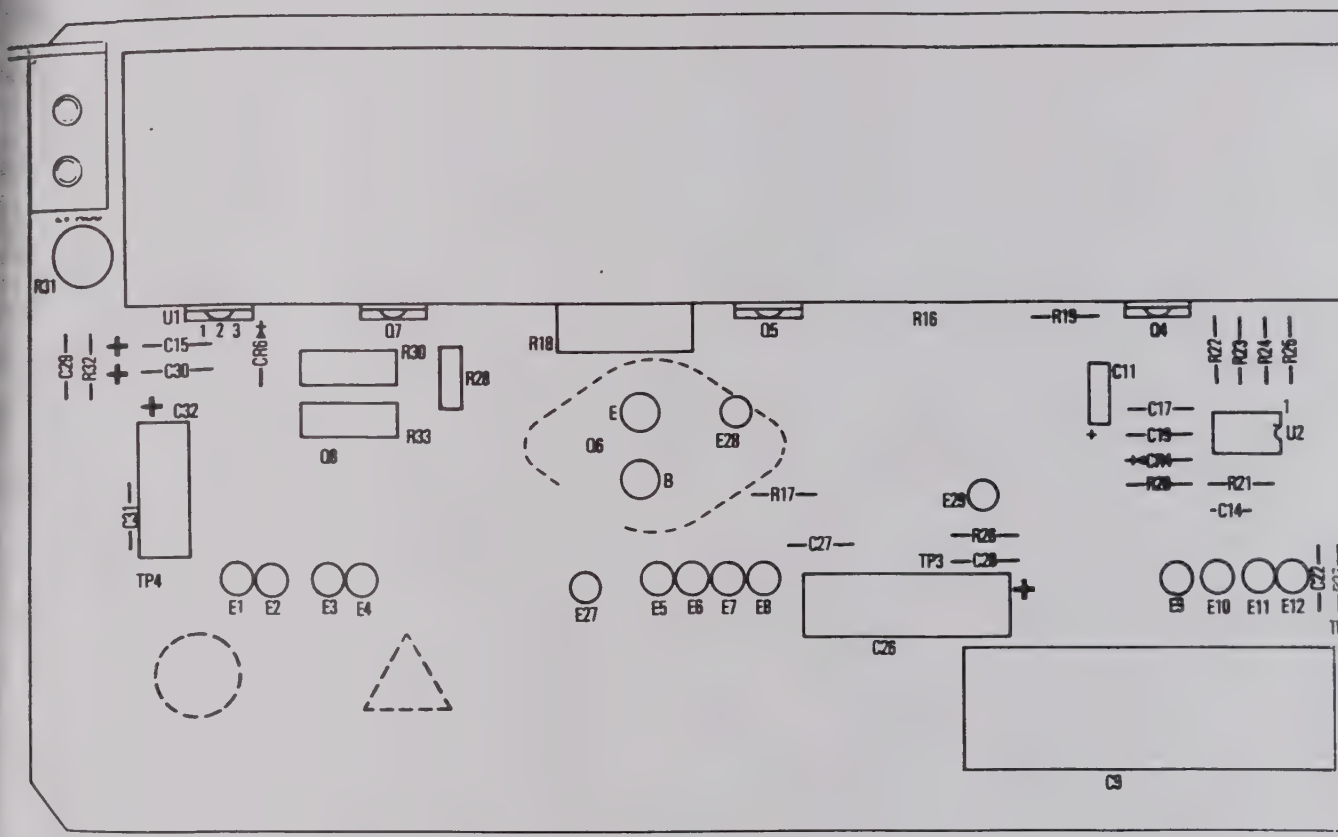

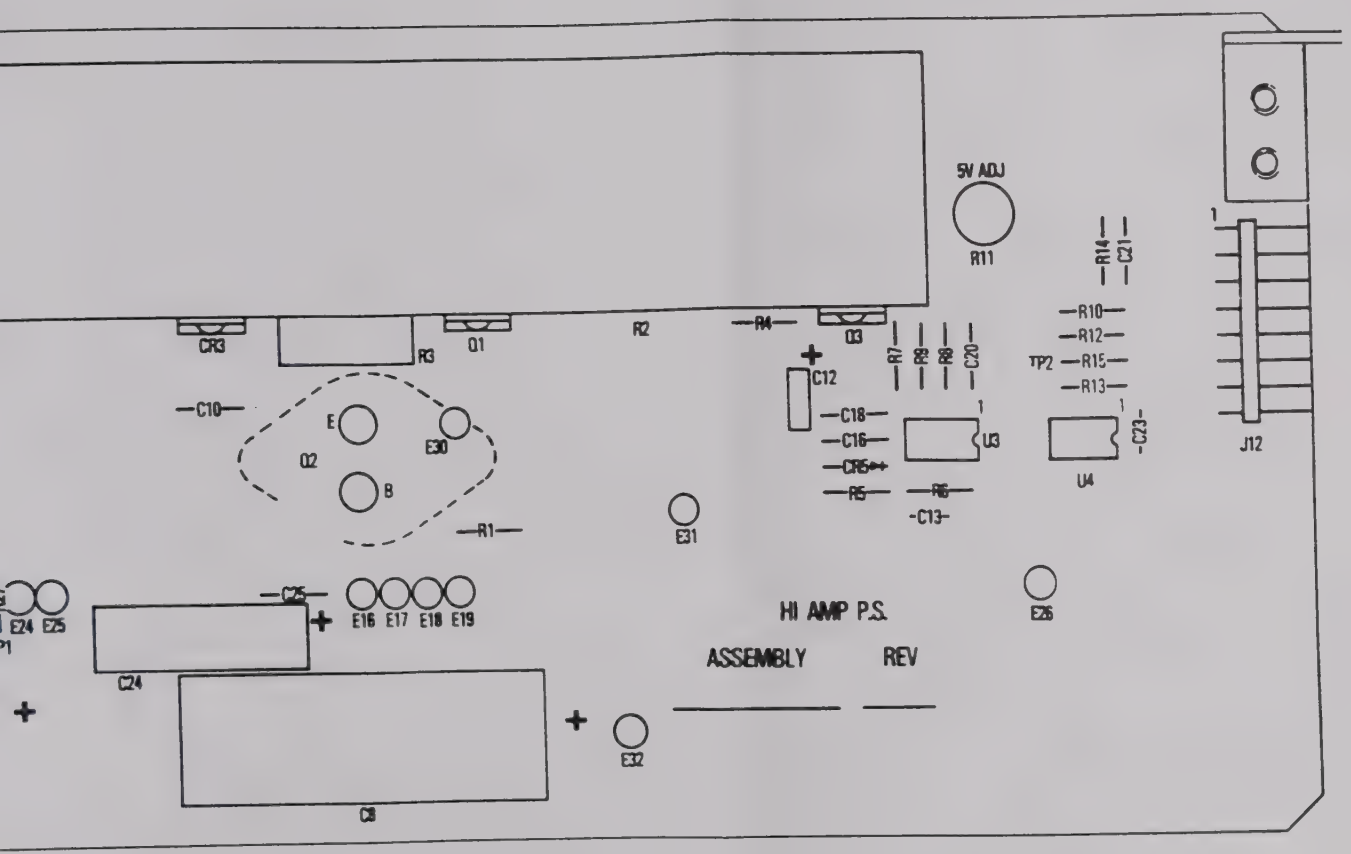

MADE FROM 0100-00-0701-3D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN / DATE	WAVETEK
MATERIAL	PROTOTYPE	TITLE: HI AMP (CURRENT) POWER SUPPLY
	RELEASE APPROV	
FINISH: WAVETEK PRINCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES .XX .030	
	DO NOT SCALE DWG	WAVETEK NO. 859 / DWG NO. 1100-00-0701 / REV D
	SCALE	CODE IDENT 23338 / SHEET 1 OF 1

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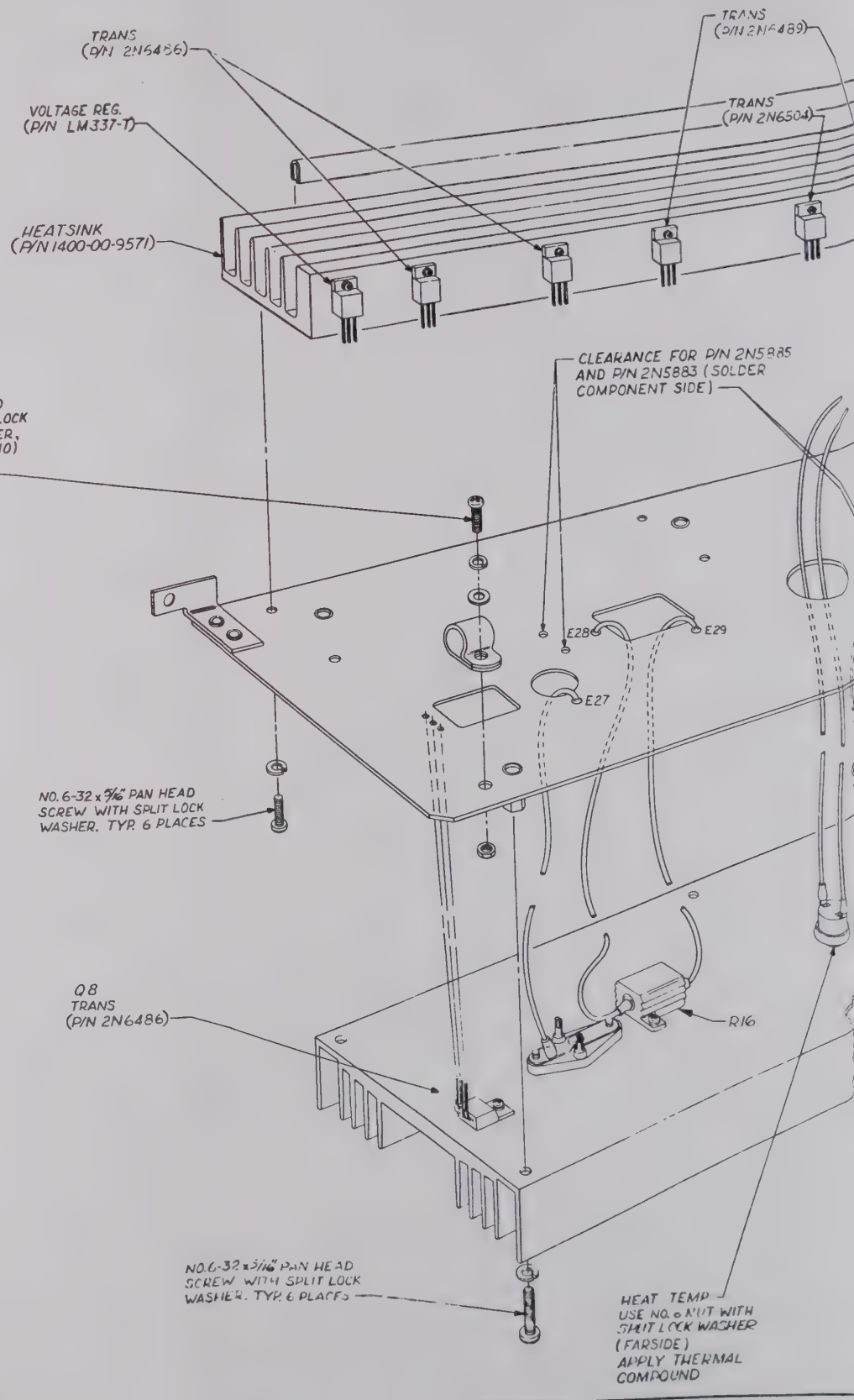
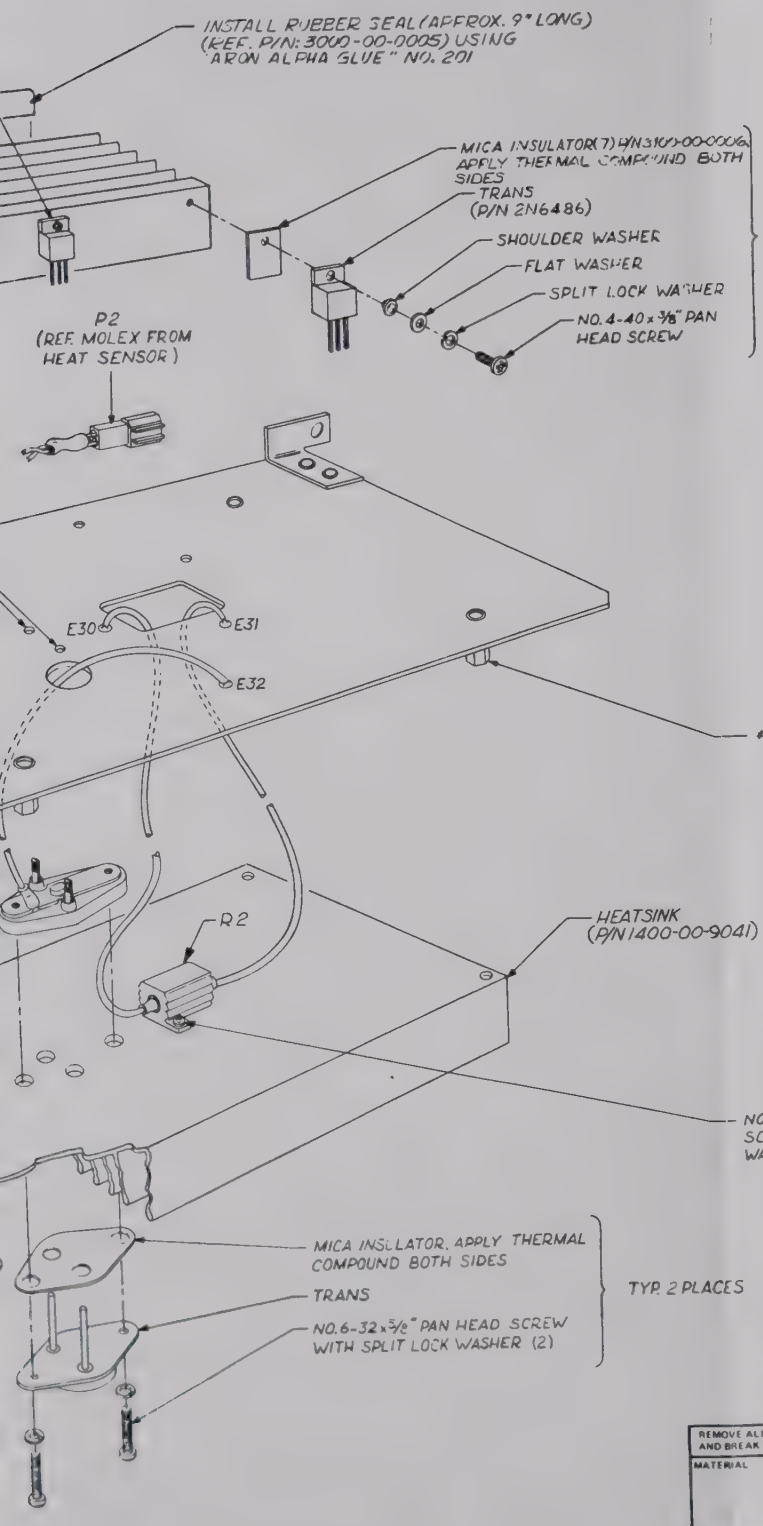


NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
F	2522	LEM	1/24/80	
G		LMK	6/11/80	
H	SEE ECN 3333 FOR SCHEMATIC			
J	3333 (4)	DC	9/30/81	



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 6-19-79	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ. ENGR		TITLE ASSEMBLY HI AMP BD.
FINISH WAVETEK PROCESS	RELEASE APPROV R. CONERO 9/8/80		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 010-0701 REV H
	SCALE	CODE IDENT 23338	SHEET 1 OF 2

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REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG, HI AMP PS
NONE	SCHEMATIC, HI AMP PS
NONE	HEATSINK, HI CURRENT REF 3200-06-0009
NONE	RETAINER, PC, LH
NONE	RETAINER, PC, RH
NONE	HEATSINK REF 3200-02-0006
C13 C14 C23 C33 C34	CAP, CER, .001MF, 1KV
C10	CAP, CER, MN, .01MF, 50V
C16 C17 C18 C19 C20 C21 C22 C25 C27 C28 C29 C31	CAP, CER, MON, .1MF, 50V
C32	CAP, ELECT, 100MF, 16V
C8 C9	CAP, ELECT, 1900MF, 15V
C24 C26	CAP, ELECT, 250MF, 16V
C11 C12 C15 C30	CAP, TANT, 1MF, 35V
NONE	POWER SUPPLY HI AMP
J12	RIGHT ANGLE CONN

WAVETEK PARTS LIST

TITLE
PCA, POWER SUPPLY HI AMP

REFERENCE DESIGNATORS	PART DESCRIPTION
P2	CONN PLUG
P16 P17	CONN HOUSING
NONE	SOCKET TO-3
NONE	PIN, MALE
NONE	PIN
NONE	CABLE CLAMP
NONE	STANDOFF, SWAGE .375 H, .250 HEX6-32, .062 MAT'L
NONE	WASHER
	RIVET 1/8X3/16L
NONE	INSULATOR, MICA
R11	POT, TRIM, 1K
R31	POT, TRIM, 200
R28	RES, C, 1/2W, 5%, 2.7
R8	RES, MF, 1/8W, 1%, 100
R14 R19 R26 R27 R4	RES, MF, 1/8W, 1%, 10
R32	RES, MF, 1/8W, 1%, 121

WAVETEK PARTS LIST

TITLE
PCA, POWER SUPPLY HI AMP

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

IG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/P1
01-00-0701	WVTK	0101-00-0701	1
03-00-0701	WVTK	0103-00-0701	1
9-9041	WVTK	1400-00-9041	1
9-9303	WVTK	1400-00-9303	1
9-9313	WVTK	1400-00-9313	1
9-9571	WVTK	1400-00-9571	1
-102 LONG LEAD	CRL	1500-01-0201	5
50-103ZA	MURAT	1500-01-0310	1
C03Z5U104Z050A	CORNG	1500-01-0405	12
0D1070016DC7	SPRAG	1500-31-0101	1
D19B0015GL4	SPRAG	1500-31-9201	2
0D257G016DF7	SPRAG	1500-32-5101	2
0D105X9035A2	SPRAG	1500-71-0502	4
9-0701	WVTK	1700-00-0701	1
7632-8	AMP	2100-02-0078	1

ASSEMBLY NO.	REV
1100-00-0701	F

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R22 R7	RES, MF, 1/8W, 1%, 12.1K	RN55D-1212F	TRW	4701-03-1212	2
R10	RES, MF, 1/8W, 1%, 1.5K	RN55D-1501F	TRW	4701-03-1501	1
R25	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R12	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	1
R23 R24 R9	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	3
R13	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
R20 R21 R5 R6	RES, MF, 1/8W, 1%, 511	RN55D-5110F	TRW	4701-03-5110	4
R15	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	1
R33	RES, WW, 3W, 1%, .3	3W, .3 OHM, 1%	DALE	4702-53-0039	1
R18 R3	RES, WW, 5W, 10%, 10	PW-5	TRW	4702-66-0100	2
R16 R2	RES, WW, 10W, 3%, .1 OHM	RH10-.1 OHM 3%	DALE	4702-77-0019	2
CR6	DIODE	1N4005	MOT	4806-01-4005	1
CR4 CR5	DIODE	1N4148	FAIR	4807-02-6666	2
Q2	TRANS	2N5883	MOT	4901-05-8830	1
Q6	TRANS	2N5885	MOT	4901-05-8850	1
Q3 Q5 Q7 Q8	TRANS	2N6486	MOT	4901-06-4860	4

WAVETEK PARTS LIST

TITLE: PCA, POWER SUPPLY HI AMP

ASSEMBLY NO.	REV
1100-00-0701	F

PAGE 3

RIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
3-06-2023	MOLEX	2100-02-0086	1
9-50-7101	MOLEX	2100-02-0087	2
P-3452-T	ROBNU	2100-03-0049	2
50629-1	AMP	2100-05-0003	2
8-50-0105	MOLEX	2100-05-0025	19
70-1505	CONCD	2800-00-0010	1
5318-3/8	USECO	2800-02-0002	6
51547F015	MOT	2800-11-0015	7
125-0406	AVDEL	2800-12-0011	4
4-21-023-106	ASHVL	3100-00-0006	7
1AR1K	BECK	4600-01-0209	1
1AR200	BECK	4600-02-0101	1
C-1/2-2R7J	STKPL	4700-25-0279	1
N55D-1000F	TRW	4701-03-1000	1
N55D-10R0F	TRW	4701-03-1009	5
N55D-1210F	TRW	4701-03-1210	1

ASSEMBLY NO.	REV
1100-00-0701	F

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q1 Q4	TRANS	2N6489	MOT	4901-06-4890	2
CR3	TRANS	2N6504	MOT	4901-06-5040	1
NONE	THERMOSTAT (180°F/83°C)	3450-22-110/T101	ELMWD	5300-00-0003	1
U1	VOLTAGE REGULATOR	LM337T	NAT	7000-03-3700	1
U2 U3	IC	LM741CN	NSC	7000-07-4100	2
U4	IC	MC 3423	MOT	7000-34-2300	1

WAVETEK PARTS LIST

TITLE: PCA, POWER SUPPLY HI AMP

ASSEMBLY NO.	REV
1100-00-0701	F

PAGE 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: PARTS LIST PCA, POWER SUPPLY HI AMP

MODEL NO	DWG NO	REV
859	1100-00-0701	F
CAGE IDENT 23338	SHEET 1 OF 1	

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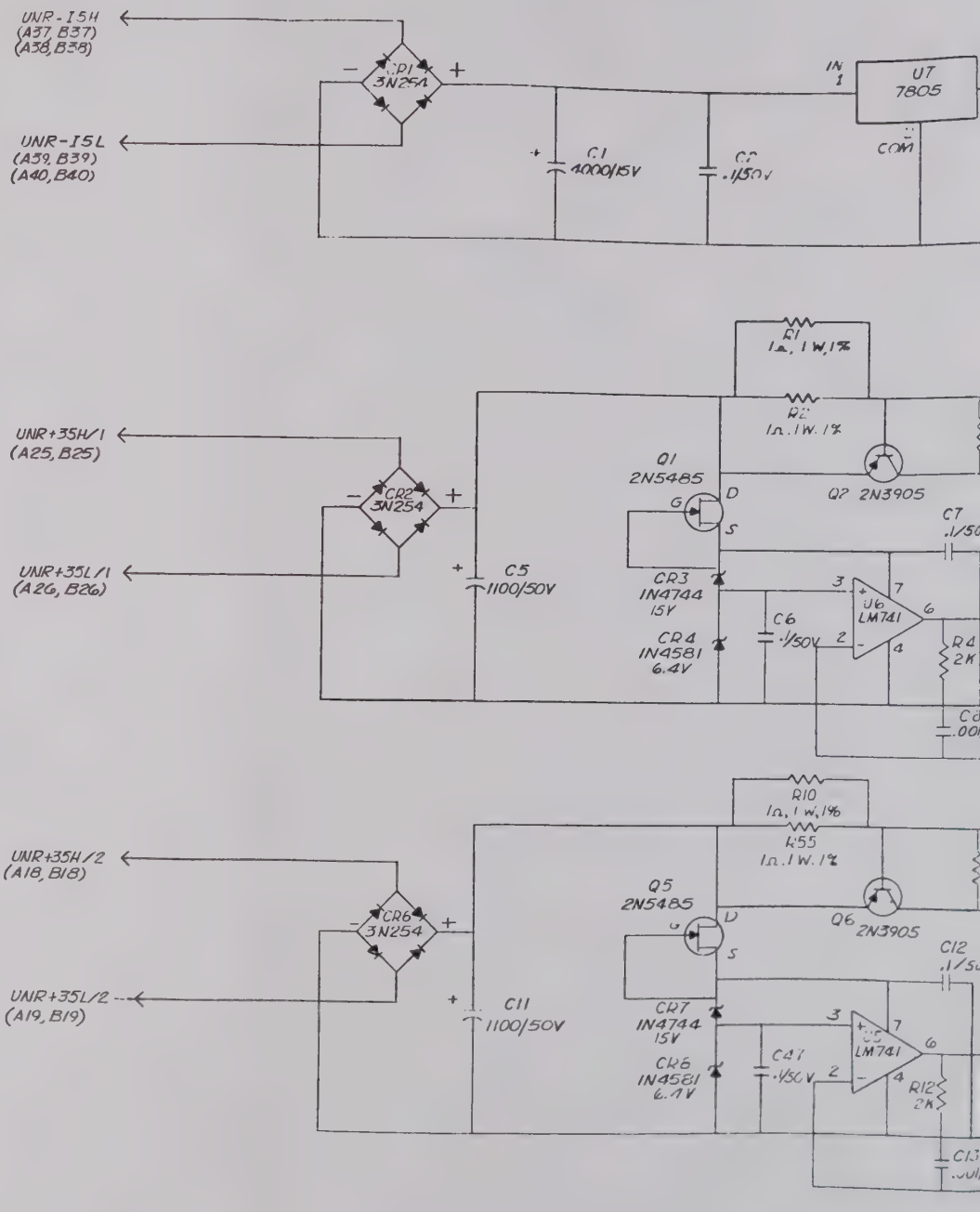
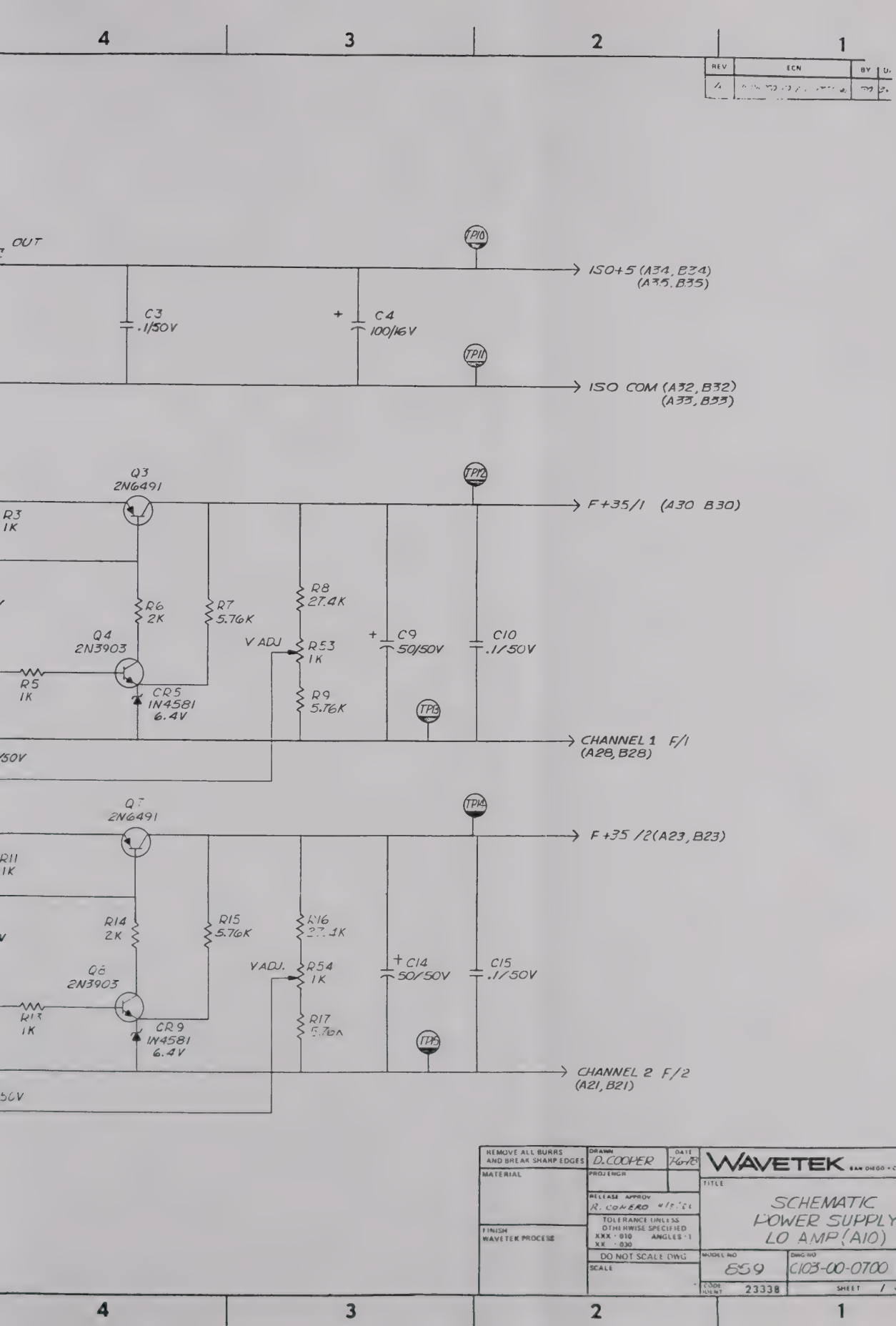


1. PARTIAL REFERENCE DESIGNATIONS SHOWN. PREFIX ASSY REF DES A10.

NOTE UNLESS OTHERWISE SPECIFIED


4
3
2
1
REV
ECN
BY
D
C
B
A
OUT
TP10
ISO+5 (A34, B34)
(A35, B35)
C3
.1/50V
+
C4
100/16V
TP11
ISO COM (A32, B32)
(A33, B33)
Q3
2N6491
TP12
F+35/1 (A30 B30)
R3
1K
R6
2K
R7
5.76K
R8
27.4K
Q4
2N3903
V ADJ
R53
1K
+
C9
50/50V
C10
.1/50V
R5
1K
CR5
IN4581
6.4V
R9
5.76K
TP13
CHANNEL 1 F/1
(A28, B28)
Q7
2N6491
TP14
F+35/2 (A23, B23)
R11
1K
R14
2K
R15
5.76K
R16
27.4K
Q8
2N3903
V ADJ.
R54
1K
+
C14
50/50V
C15
.1/50V
R17
5.76K
CR9
IN4581
6.4V
TP15
CHANNEL 2 F/2
(A21, B21)
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN
D. COOPER
DATE
PROJ ENGR
RELEASE APPROV
R. CONERO
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1°
XX ± .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC
POWER SUPPLY
LO AMP (A10)
MODEL NO
859
DWG NO
C103-00-0700
REV
B
CODE IDENT NO
23338
SHEET 1 OF 2

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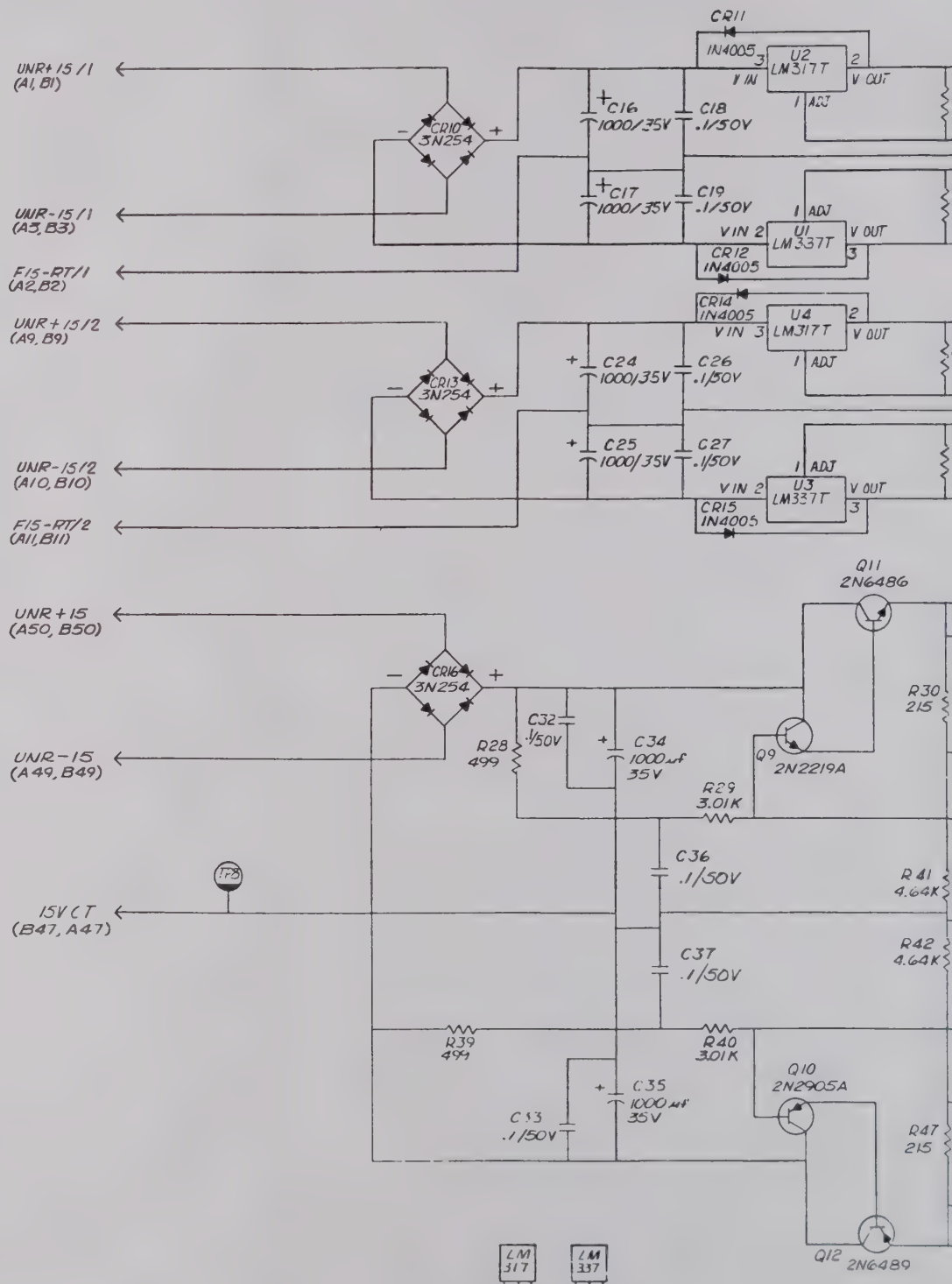
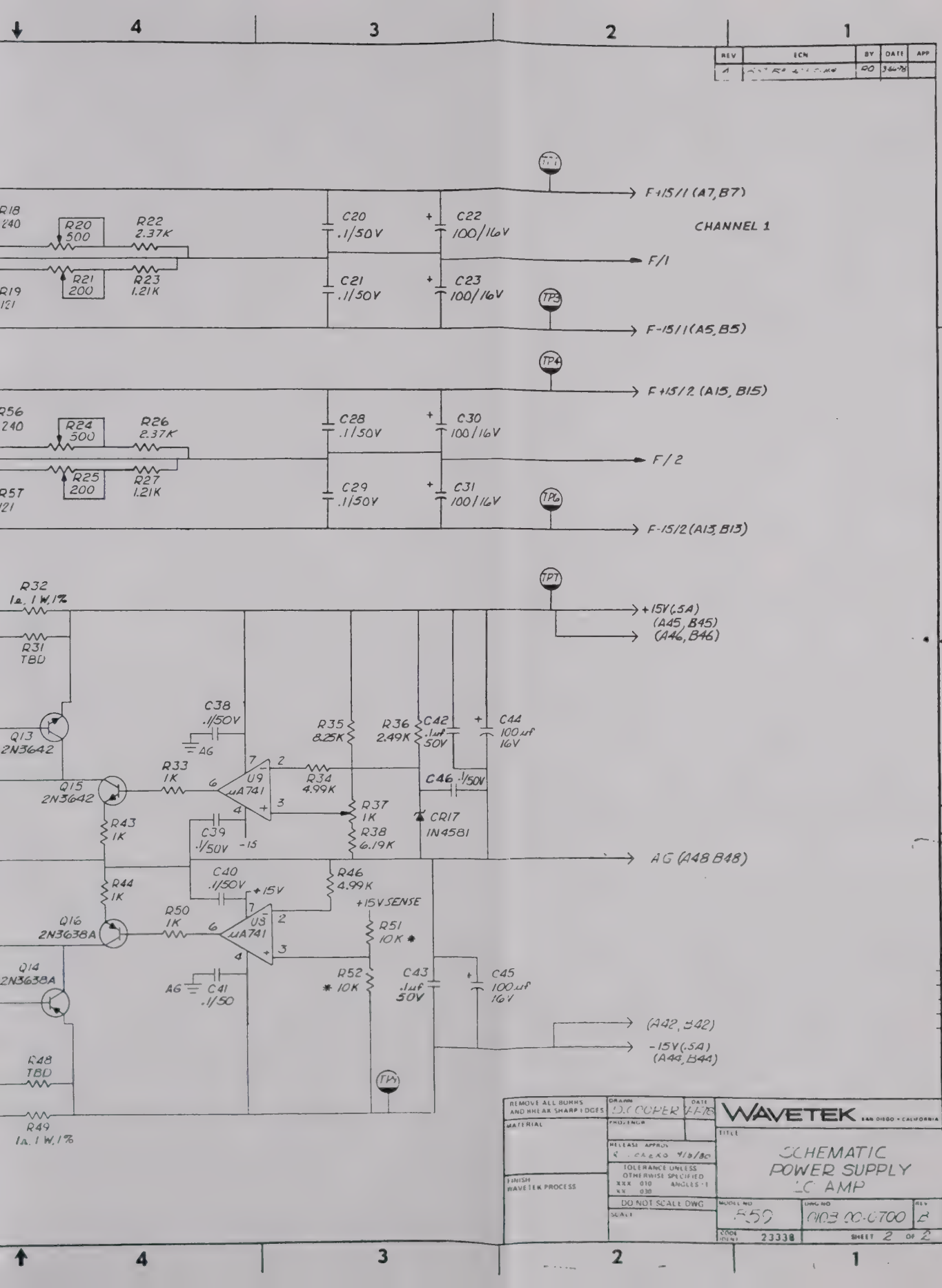


1. * = MATCHED SET OF ICs

NOTE UNLESS OTHERWISE SPECIFIED



REV
ECN
BY
DATE
APP
F+15/1 (A7,B7)
CHANNEL 1
F/1
F-15/1 (A5,B5)
F+15/2 (A15,B15)
F/2
F-15/2 (A13,B13)
+15V(.5A)
(A45,B45)
(A46,B46)
AG (A48 B48)
(A42,B42)
-15V(.5A)
(A44,B44)
R18 240
R20 500
R22 2.37K
R21 200
R23 1.21K
R19 121
C20 .1/50V
C22 100/16V
C21 .1/50V
C23 100/16V
R56 240
R24 500
R26 2.37K
R25 200
R27 1.21K
R57 121
C28 .1/50V
C30 100/16V
C29 .1/50V
C31 100/16V
R32 1Ω, 1W, 1%
R31 TBD
Q13 2N3642
Q15 2N3642
Q16 2N3638A
Q14 2N3638A
R48 TBD
R49 1Ω, 1W, 1%
R33 1K
R43 1K
R44 1K
R50 1K
C38 .1/50V
AG
U9 μA741
C39 .1/50V
-15
C40 .1/50V
+15V
U8 μA741
C41 .1/50
R35 8.25K
R34 4.99K
R37 1K
R38 6.19K
R46 4.99K
R36 2.49K
C42 .1μf 50V
C44 100μf 16V
C46 .1/50V
CR17 1N4581
+15V SENSE
R51 10K *
R52 * 10K
C43 .1μf 50V
C45 100μf 16V
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D.COOPER
DATE
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX .010 ANGLES ±1
XX .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC
POWER SUPPLY
LC AMP
MODEL NO 559
DWG NO 0103 00-0700
REV B
CODE IDENT 23338
SHEET 2 OF 2

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REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG, LO AMP PS
NONE	SCHEMATIC, LO AMP PS
NONE	HEATSINK REF 3200-02-0006
C13 C8	CAP, CER, .001MF, 3KV
C10 C12 C15 C18 C19 C2 C20 C21 C26 C27 C28 C29 C3 C32 C33 C36 C37 C38 C39 C40 C41 C42 C43 C46 C47 C6 C7	CAP, CER, MON, 1MF, 50V
C22 C23 C30 C31 C4 C44 C45	CAP, ELECT, 100MF, 16V
C16 C17 C24 C25	CAP, ELECT, 1000MF/35V RADIAL LEAD, SP .30
C34 C35	CAP, ELECT, 1000MF, 35V
C11 C5	CAP, ELECT, 1100MF, 50V
C1	CAP, ELECT, 4000MF, 15V
C14 C9	CAP, ELECT, 50MF, 50V
NONE	POWER SUPPLY LO AMP
TP1 TP10 TP11 TP12 TP13 TP14 TP15 TP3 TP4 TP6 TP7 TP8 TP9	BUSS BAR STANDOFF

WAVETEK PARTS LIST	TITLE: PCA, POWER SUPPLY LO AMP

REFERENCE DESIGNATORS	PART DESCRIPTION
2	PC BD EJECTOR
NONE	TRANSIPAD
NONE	WASHER
NONE	INSULATOR, MICA
R37 R53 R54	POT, TRIM, 1K
R21 R25	POT, TRIM, 200
R20 R24	POT, TRIM, 500
R11 R13 R3 R33 R43 R44 R5 R50	RES, MF, 1/8W, 1%, 1K
R19 R57	RES, MF, 1/8W, 1%, 121
R23 R27	RES, MF, 1/8W, 1%, 1 21K
R12 R14 R4 R6	RES, MF, 1/8W, 1%, 2K
R30 R47	RES, MF, 1/8W, 1%, 215
R22 R26	RES, MF, 1/8W, 1%, 2 37K
R18 R56	RES, MF, 1/8W, 1%, 240
R36	RES, MF, 1/8W, 1%, 2 49K
R16 R8	RES, MF, 1/8W, 1%, 27 4K

WAVETEK PARTS LIST	TITLE: PCA, POWER SUPPLY LO AMP

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
0101-00-0700	WVTK	0101-00-0700	1
0103-00-0700	WVTK	0103-00-0700	1
859-9561	WVTK	1400-00-9561	1
DD30-102	CRL	1500-01-0205	2
CAC03Z5U104Z050A	CORNG	1500-01-0405	27
500D1070016DC7	SPRAG	1500-31-0101	7
CRE-SERIES-1000/35	CAPAR	1500-31-0202	4
39D108G035GL6	SPRAG	1500-31-0212	2
39D118G050MP4	SPRAG	1500-31-1203	2
TC0402U015N1L	MAL	1500-34-0211	1
500D5060050DD7	SPRAG	1500-35-0003	2
859-0700	WVTK	1700-00-0700	1
2110-001	ARTWR	2100-05-0024	13

ASSEMBLY NO.	REV
1100-00-0700	

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R29 R40	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	2
R41 R42	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	2
R28 R39	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	2
R34 R46	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	2
R15 R17 R7 R9	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	4
R38	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R35	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R1 R10 R2 R32 R49 R55	RES, WW, 1W, 1%, 1	RS1A 1 OHM 1%	DALE	4702-33-1009	6
R51 R52	RES, SET, 2-10K, 1/8W QTY 2: 4701-03-1002	142-501-64A	WVTK	4789-00-0019	1
CR17 CR4 CR5 CR8 CR9	DIODE	1N4581	MICRO	4801-01-4581	5
CR3 CR7	DIODE	1N4744	MOT	4801-01-4744	2
CR1 CR10 CR13 CR16 CR2 CR6	DIODE	3N254	MOT	4801-02-0254	6
CR11 CR12 CR14 CR15	DIODE	1N4005	MOT	4806-01-4005	4
Q9	TRANS	2N2219A	NSC	4901-02-2191	1
Q10	TRANS	2N2905A	NSC	4901-02-9051	1
Q14 Q16	TRANS	2N3638A	CARTR	4901-03-6381	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, POWER SUPPLY LO AMP	1100-00-0700	

PAGE 3

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
103 RED	CALMK	2800-07-0010	2
10123N	METRS	2800-11-0003	2
851547F015	MOT	2800-11-0015	9
64-21-023-106	ASHVL	3100-00-0006	9
91AR1K	BECK	4600-01-0209	3
91AR200	BECK	4600-02-0101	2
91AR500	BECK	4600-05-0104	2
RN55D-1001F	TRW	4701-03-1001	8
RN55D-1210F	TRW	4701-03-1210	2
RN55D-1211F	TRW	4701-03-1211	2
RN55D-2001F	TRW	4701-03-2001	4
RN55D-2150F	TRW	4701-03-2150	2
RN55D-2371F	TRW	4701-03-2371	2
RN55D-2400F	MEPCO	4701-03-2400	2
RN55D-2491F	TRW	4701-03-2491	1
RN55D-2742F	TRW	4701-03-2742	2

ASSEMBLY NO.	REV
1100-00-0700	

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q13 Q15	TRANS	2N3642	FAIR	4901-03-6420	2
Q4 Q8	TRANS	2N3903	NSC	4901-03-9030	2
Q2 Q6	TRANS	2N3905	ITT	4901-03-9050	2
Q1 Q5	TRANS	2N5485	MOT	4901-05-4850	2
Q11	TRANS	2N6486	MOT	4901-06-4860	1
Q12	TRANS	2N6489	MOT	4901-06-4890	1
Q3 Q7	TRANS	2N6491	MOT	4901-06-4910	2
U2 U4	IC	LM317T	NSC	7000-03-1700	2
U1 U3	VOLTAGE REGULATOR	LM337T	NAT	7000-03-3700	2
U5 U6 U8 U9	IC	LM741CN	NSC	7000-07-4100	4
U7	VOLTAGE REGULATOR	MA7805UC	FAIR	8000-78-0500	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, POWER SUPPLY LO AMP	1100-00-0700	

PAGE 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, POWER SUPPLY LO AMP
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 1100-00-0700 REV F
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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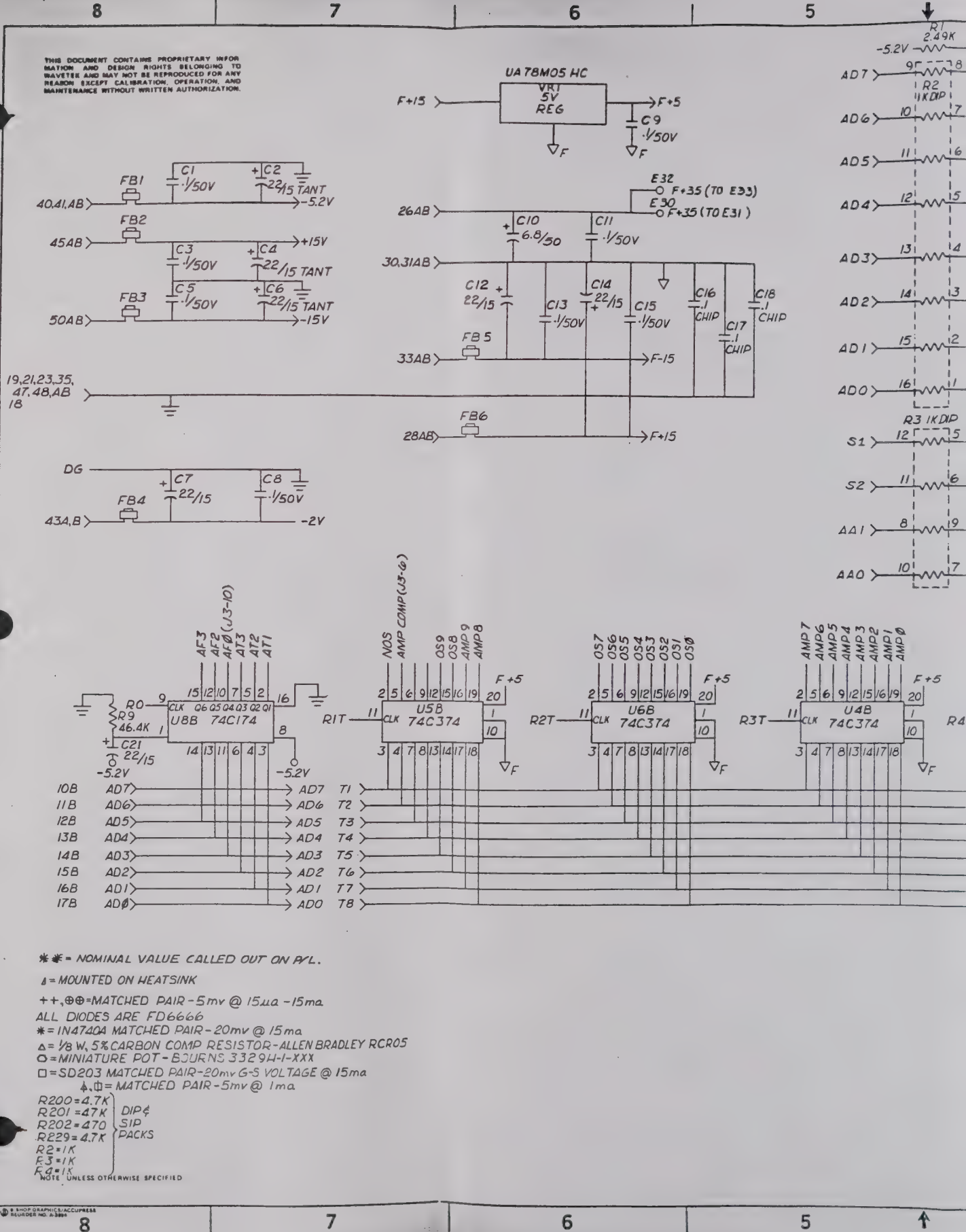

** = NOMINAL VALUE CALLED OUT ON P/L.

♦ = MOUNTED ON HEATSINK

++, ⊕⊕ = MATCHED PAIR - 5mv @ 15μa - 15ma

ALL DIODES ARE FD6666

✱ = IN4740A MATCHED PAIR - 20mv @ 15ma

△ = 1/8 W, 5% CARBON COMP RESISTOR - ALLEN BRADLEY RCR05

○ = MINIATURE POT - BOURNS 3329H-1-XXX

□ = SD203 MATCHED PAIR - 20mv G-S VOLTAGE @ 15ma

♦, ⊕ = MATCHED PAIR - 5mv @ 1ma

R200 = 4.7K
R201 = 47K
R202 = 470
R229 = 4.7K
R2 = 1K
R3 = 1K
R4 = 1K

DIP & SIP PACKS

NOTE UNLESS OTHERWISE SPECIFIED

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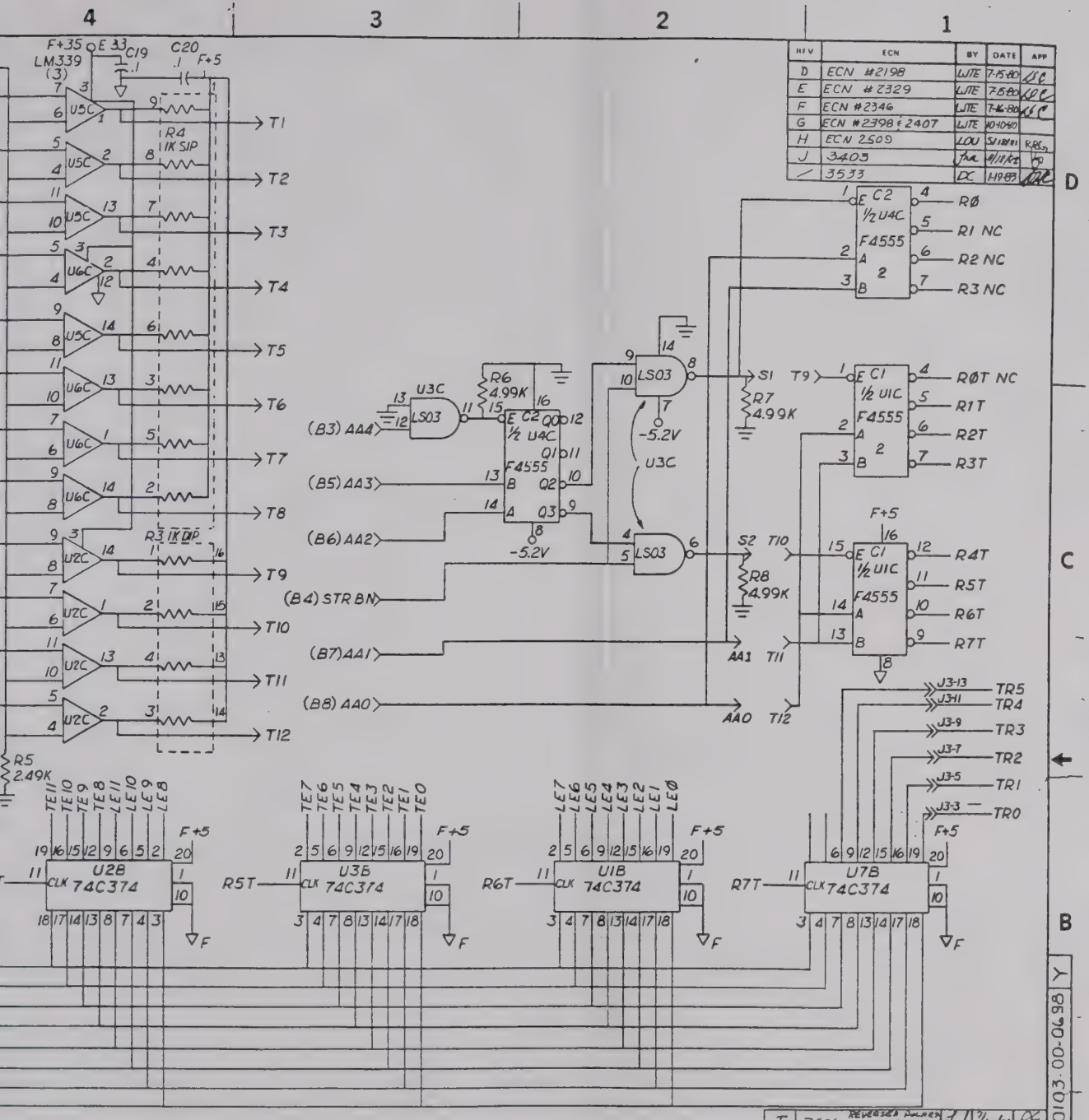

REV	ECN	BY	DATE	APP
D	ECN #2198	WJTE	7-15-80	[illegible]
E	ECN #2329	WJTE	7-15-80	[illegible]
F	ECN #2346	WJTE	7-16-80	[illegible]
G	ECN #2398 & 2407	WJTE	10-10-80	
H	ECN 2509	LOU	5/18/81	RBG
J	3403	[illegible]	4/18/82	[illegible]
/	3533	DC	1-19-83	[illegible]

T	7556 REVERSED POLARITY ON K1, 2, 4, 5, 6	[illegible]	7/10/86	[illegible]
S	7492	RG	6/4/86	[illegible]
R	7130	RO	2-25-86	[illegible]
Q	4928	SC	8-30-85	[illegible]
P	ECN 4825	JK	5-31-85	[illegible]
N	ECN 4337	RO	9-11-84	[illegible]
M	ECN 4334	RO	[illegible]	[illegible]
L	ECN 4137	RO	1/84	[illegible]
K	3764	[illegible]	5-11-83	
REV	ECN	BY	DATE	APP

Y	# 8221	N.C. #2717	4-28-87	SS
W	7755	BR	10/30/6	[illegible]
V	7748	BR	10/27/6	[illegible]
U	7650	RO	9-5-86	[illegible]

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN S. CHERMACK DATE 10-10-73

PROJ ENGR [illegible]

RELEASE APPROV R. CONERO 4/8/80

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

SCHEMATIC POWER AMPLIFIER BD.

MODEL NO 359 | DWG NO 0103-00-0698 | REV Y

CODE IDENT 23338 | SHEET 1 OF 5

0103-00-0698 Y

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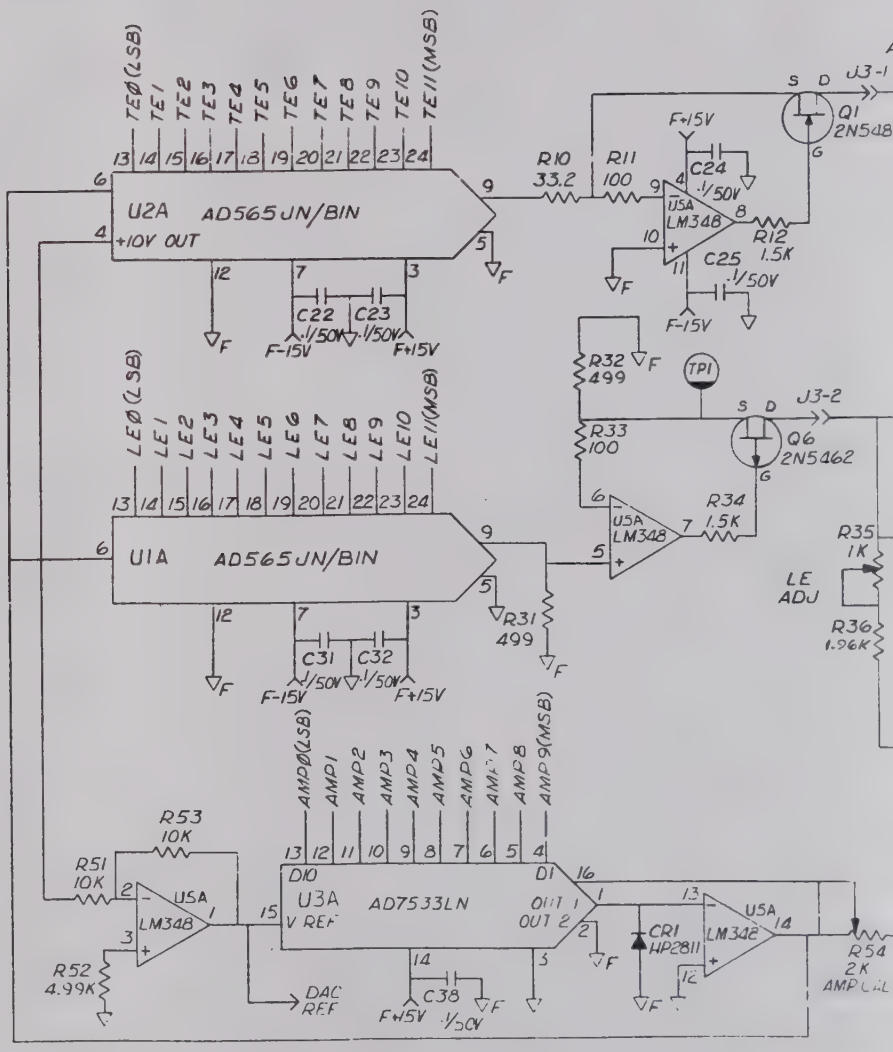
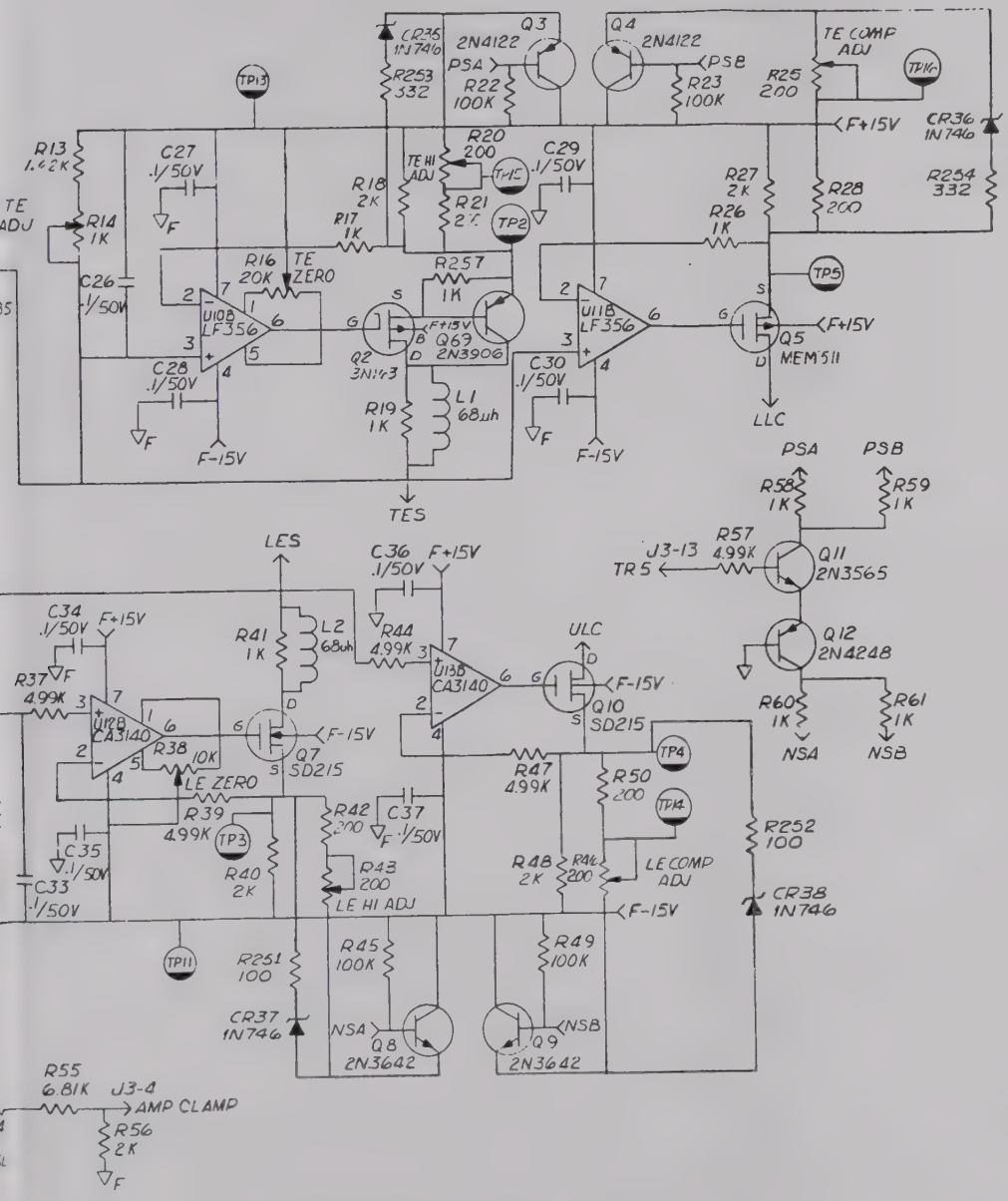


NOTE UNLESS OTHERWISE SPECIFIED



REMOVE ALL BURRS AND SHARP EDGES	DRAWN S.CHERMACK	DATE 12-[illegible]-79	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC POWER AMPLIFIER B.D.
	RELEASE APPROV R. [illegible] 4/3/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO [illegible]	DWG NO 0103-00-0698 REV W
	SCALE	CODE IDENT 23338	SHEET 2 OF 5

0103-00-0698

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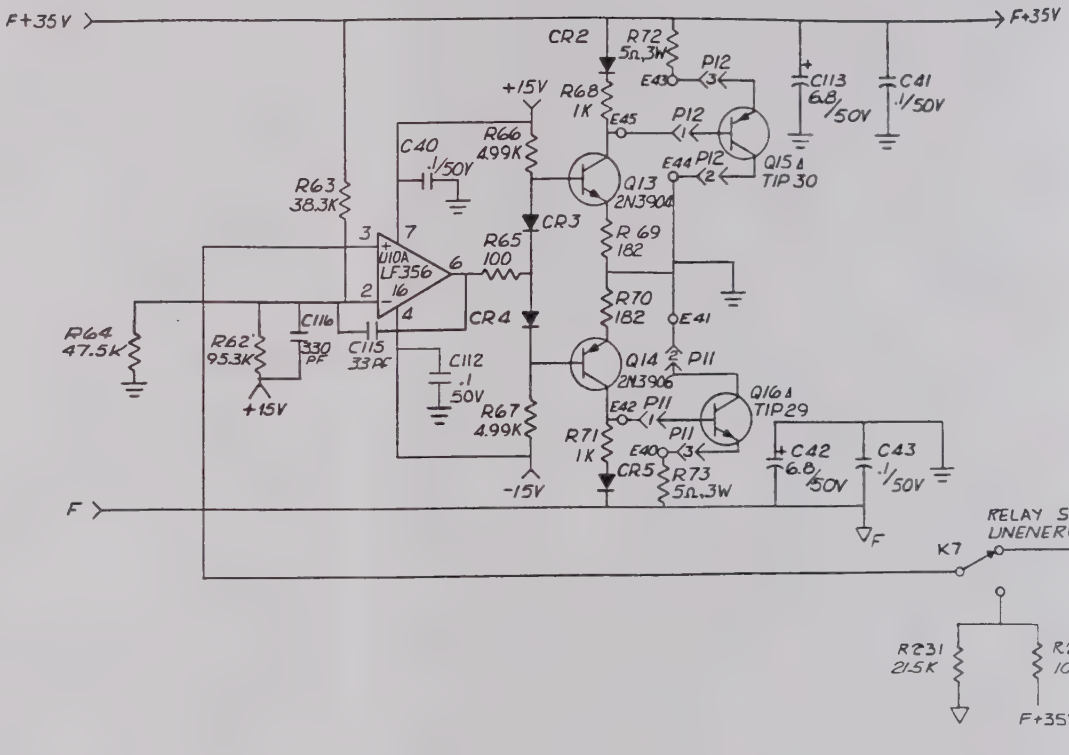
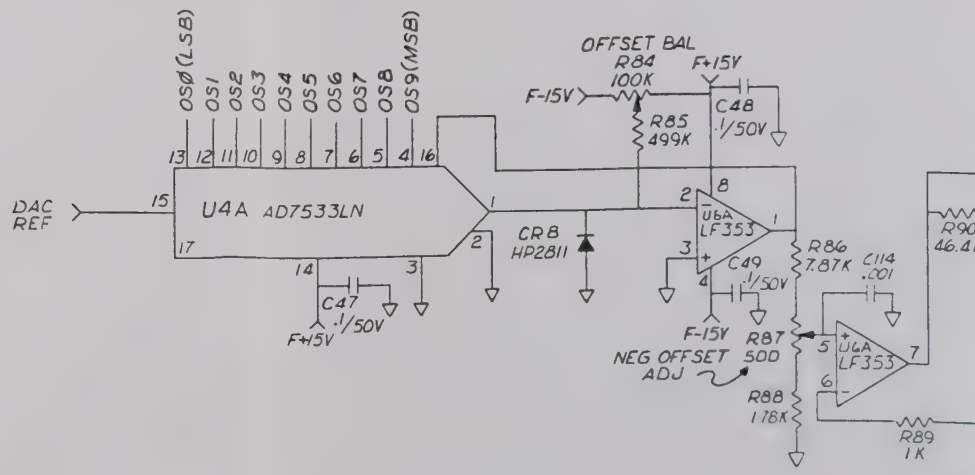
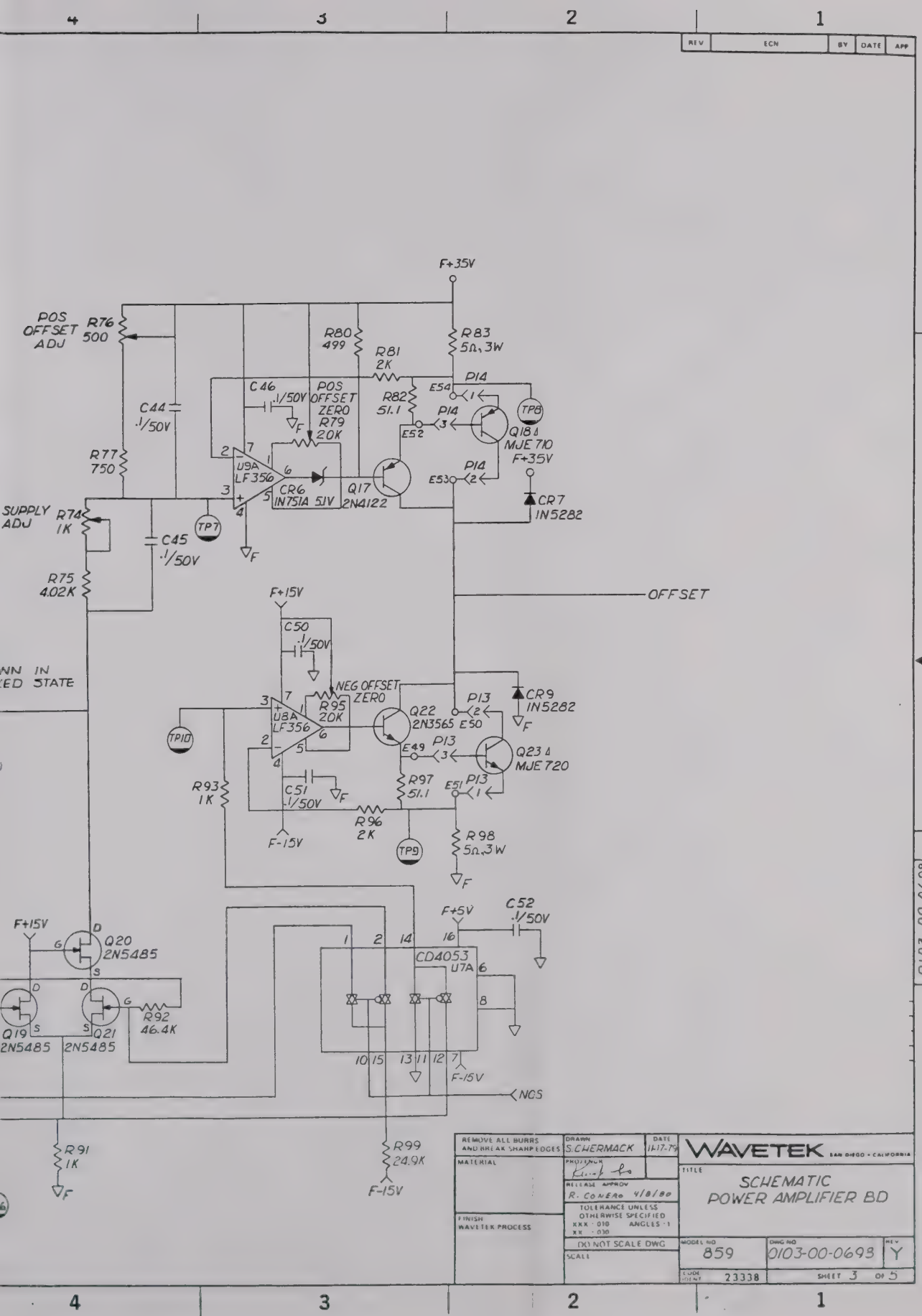




NOTE UNLESS OTHERWISE SPECIFIED


REV
ECN
BY
DATE
APP
F+35V
POS OFFSET ADJ
R76 500
R80 499
R81 2K
R83 5Ω, 3W
C46 .1/50V
POS OFFSET ZERO R79 20K
R82 51.1
P14
E54
TP8
Q18 MJE 710
F+35V
C44 .1/50V
R77 750
U9A LF356
CR6 IN751A 5.1V
Q17 2N4122
E52
E53
CR7 IN5282
SUPPLY ADJ
R74 1K
TP7
C45 .1/50V
R75 4.02K
OFFSET
F+15V
C50 .1/50V
NEG OFFSET ZERO
R95 20K
U8A LF356
Q22 2N3565
P13
E50
CR9 IN5282
TP10
E49
Q23 MJE 720
R93 1K
C51 .1/50V
R97 51.1
E51
R96 2K
F-15V
TP9
R98 5Ω, 3W
F+5V
C52 .1/50V
F+15V
Q20 2N5485
CD4053 U7A
R92 46.4K
Q19 2N5485
Q21 2N5485
NCS
R91 1K
R99 24.9K
F-15V
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S.CHERMACK
DATE 11-17-79
PROJ ENG
RELEASE APPROV R. CONERO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC POWER AMPLIFIER BD
MODEL NO 859
DWG NO 0103-00-0693
REV Y
CODE IDENT 23338
SHEET 3 OF 5
0103-00-0698

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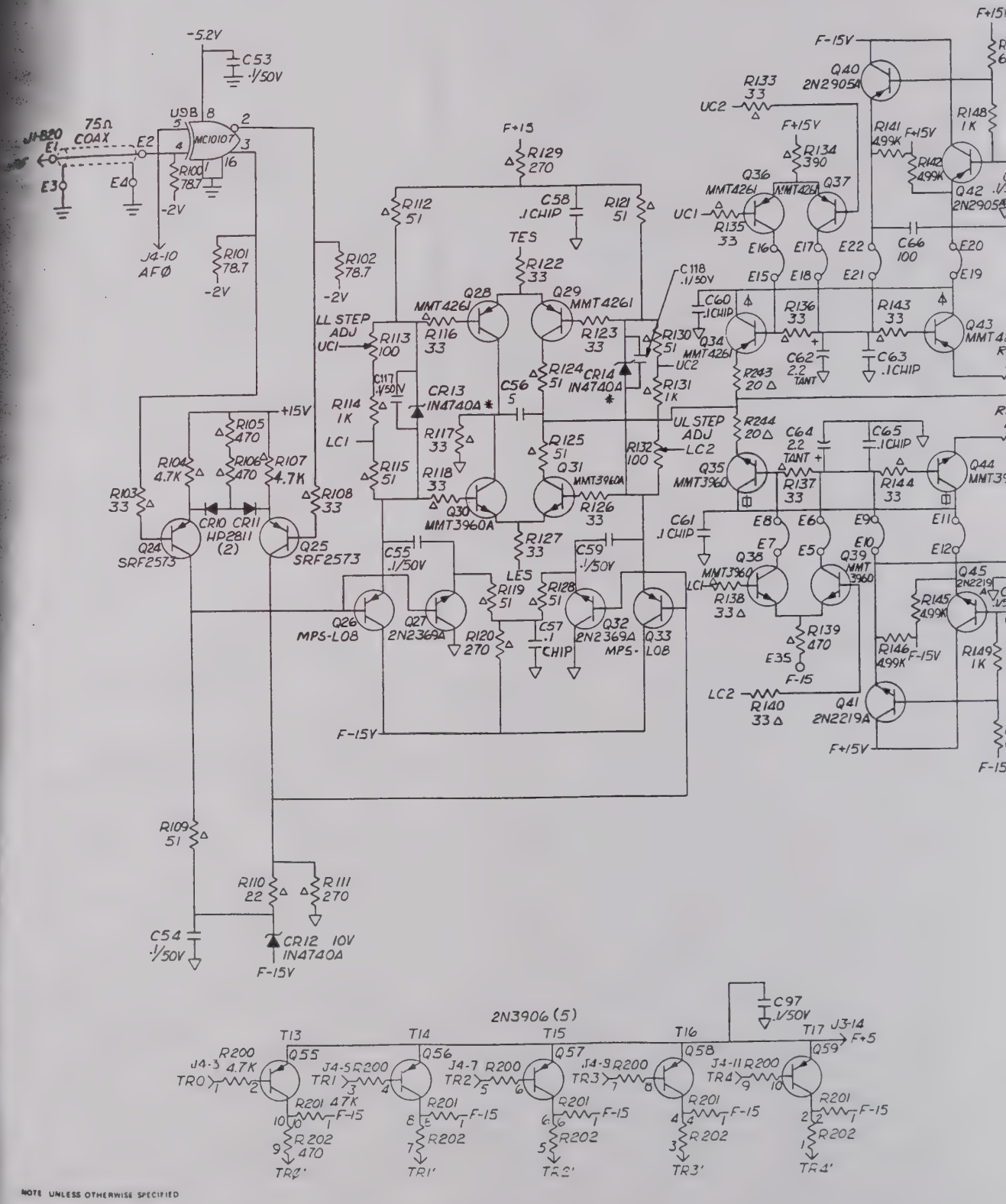
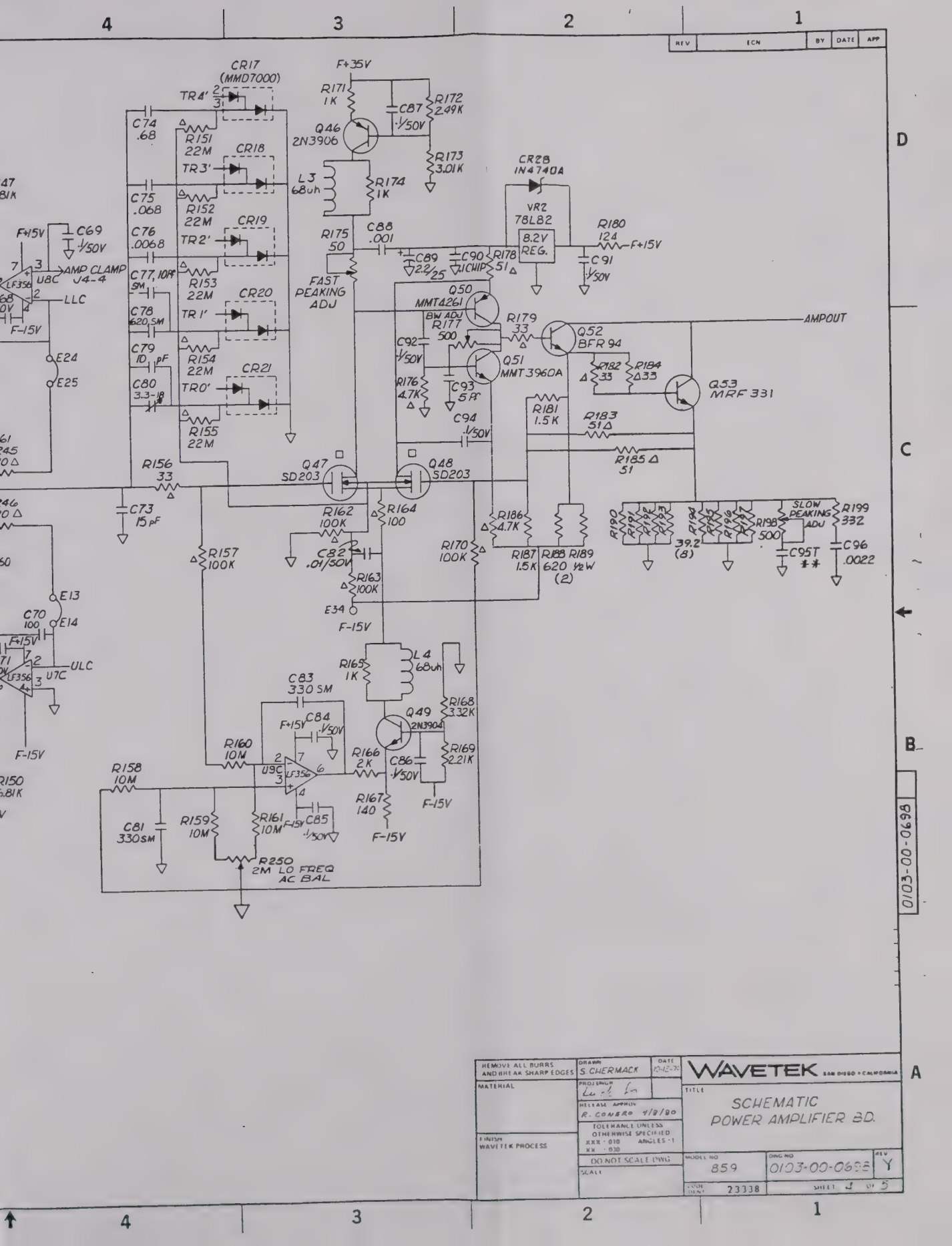
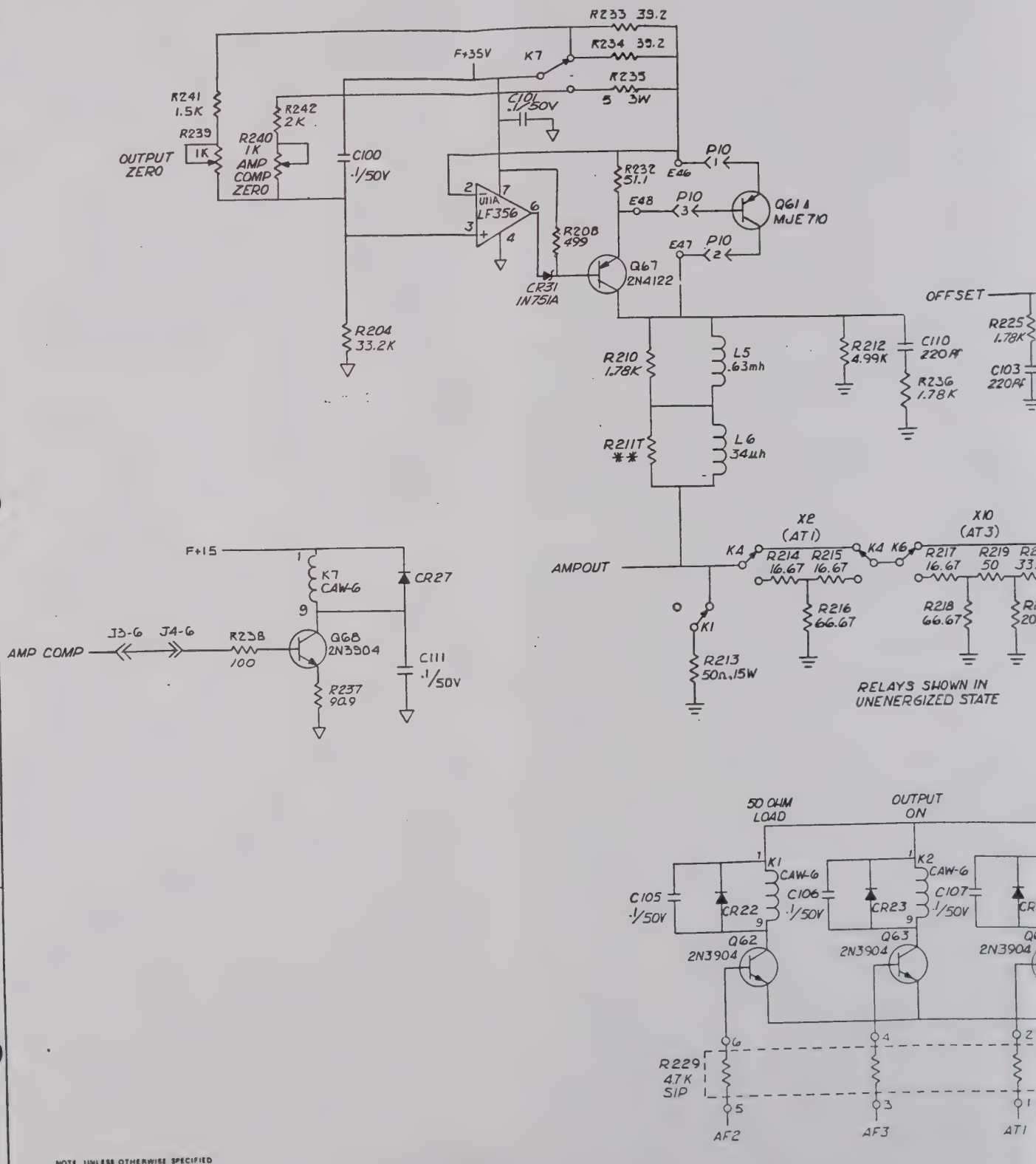


NOTE UNLESS OTHERWISE SPECIFIED

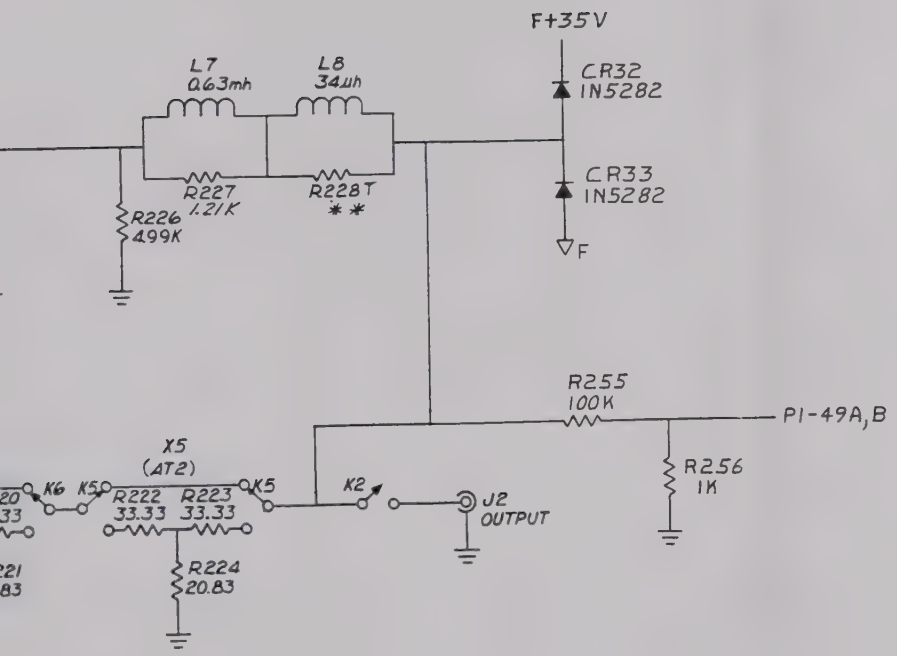


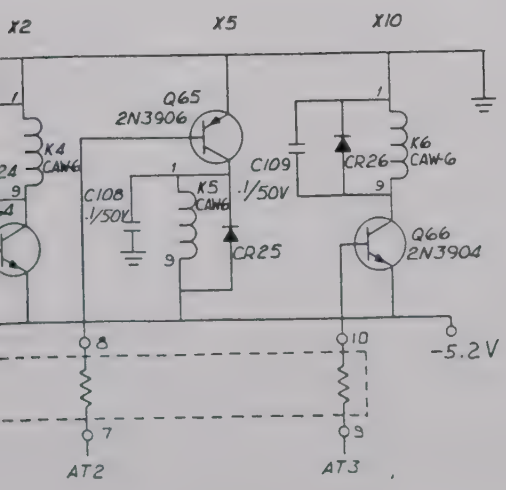
CR17 (MMD7000)
TR4'
C74 .68
R151 22M
CR18
TR3'
C75 .068
R152 22M
CR19
TR2'
C76 .0068
C77, 10pF SM
R153 22M
CR20
TR1'
C78 620 SM
C79 10 pF
R154 22M
CR21
TR0'
C80 3.3-18
R155 22M
F+35V
R171 1K
C87 .1/50V
R172 2.49K
Q46 2N3906
R173 3.01K
L3 68uh
R174 1K
R175 50
C88 .001
FAST PEAKING ADJ
CR28 1N4740A
VR2 78L82
8.2V REG.
R180 124
F+15V
C89 2.2/25
C90 .1CHIP
R178 51
C91 .1/50V
Q50 MMT4261
BW ADJ R177 500
R179 33
Q52 BFR 94
AMPOUT
C92 .1/50V
Q51 MMT3960A
R176 4.7K
C93 5pF
R182 33
R184 33
Q53 MRF 331
R181 1.5K
R183 51
C94 .1/50V
R185 51
R156 33
Q47 SD203
Q48 SD203
C73 15pF
R162 100K
R164 100
R186 4.7K
R170 100K
R187 1.5K
R188 620 1/2W (2)
R189
R190 R191 R192 R193 R194 R195 R196 R197 39.2 (8)
R198 500
SLOW PEAKING ADJ
R199 332
C95T **
C96 .0022
R157 100K
C82 .01/50V
R163 100K
E34
F-15V
R165 1K
L4 68uh
C83 330 SM
C84 .1/50V
Q49 2N3904
R168 3.32K
R169 2.21K
R160 10M
U9C LF356
R166 2K
C86 .1/50V
R158 10M
R167 140
C81 330SM
R159 10M
R161 10M
C85 .1/50V
R250 2M LO FREQ AC BAL
F+15V
C69 .1/50V
AMP CLAMP J4-4
U8C LF356
LLC
F-15V
E24
E25
E13
E14
C70 100
U7C LF356
ULC
0103-00-0698
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S. CHERMACK
DATE 10-12-79
PROJ ENGR
RELEASE APPROV R. CONERO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC POWER AMPLIFIER BD.
MODEL NO 859
DWG NO 0103-00-0698
REV Y
CODE IDENT 23338
SHEET 4 OF 5

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.



NOTE UNLESS OTHERWISE SPECIFIED

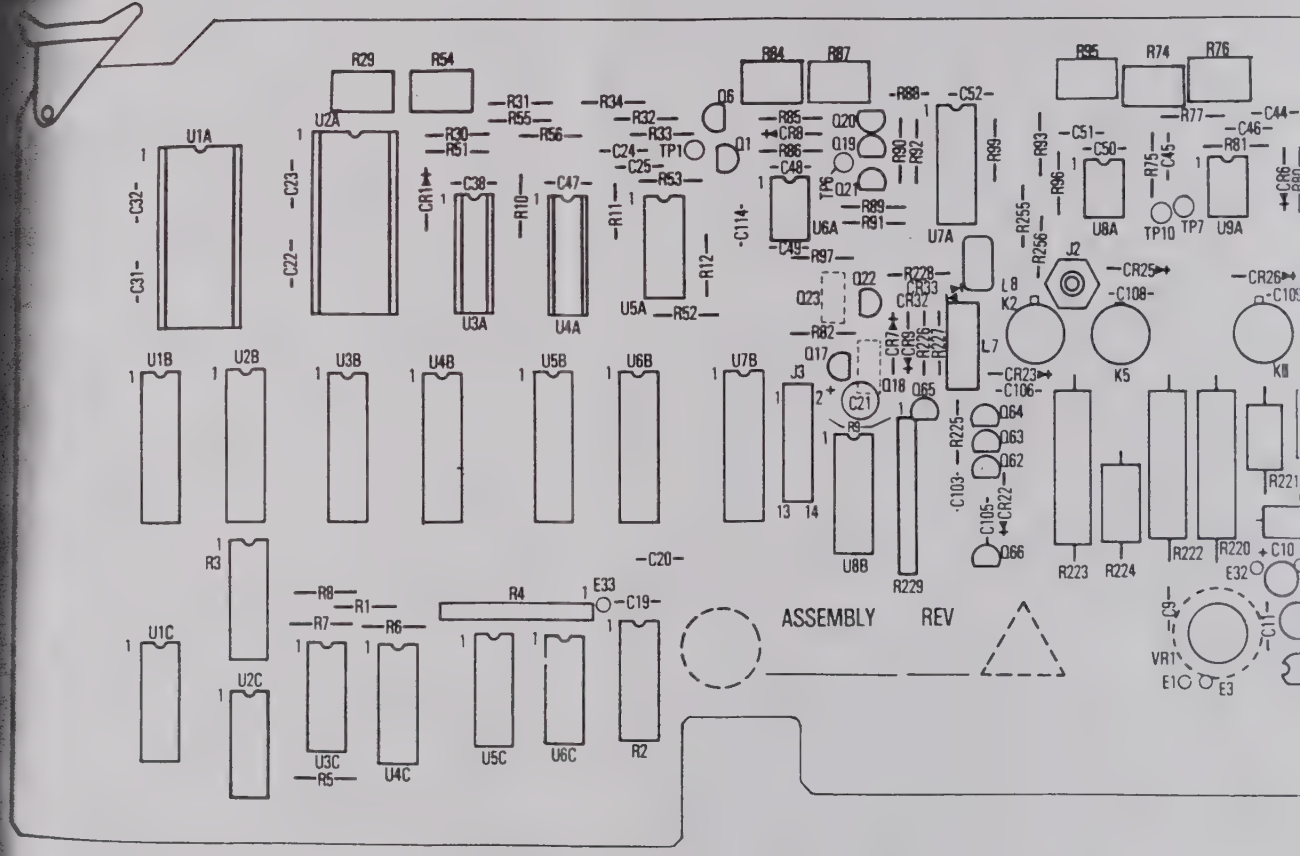


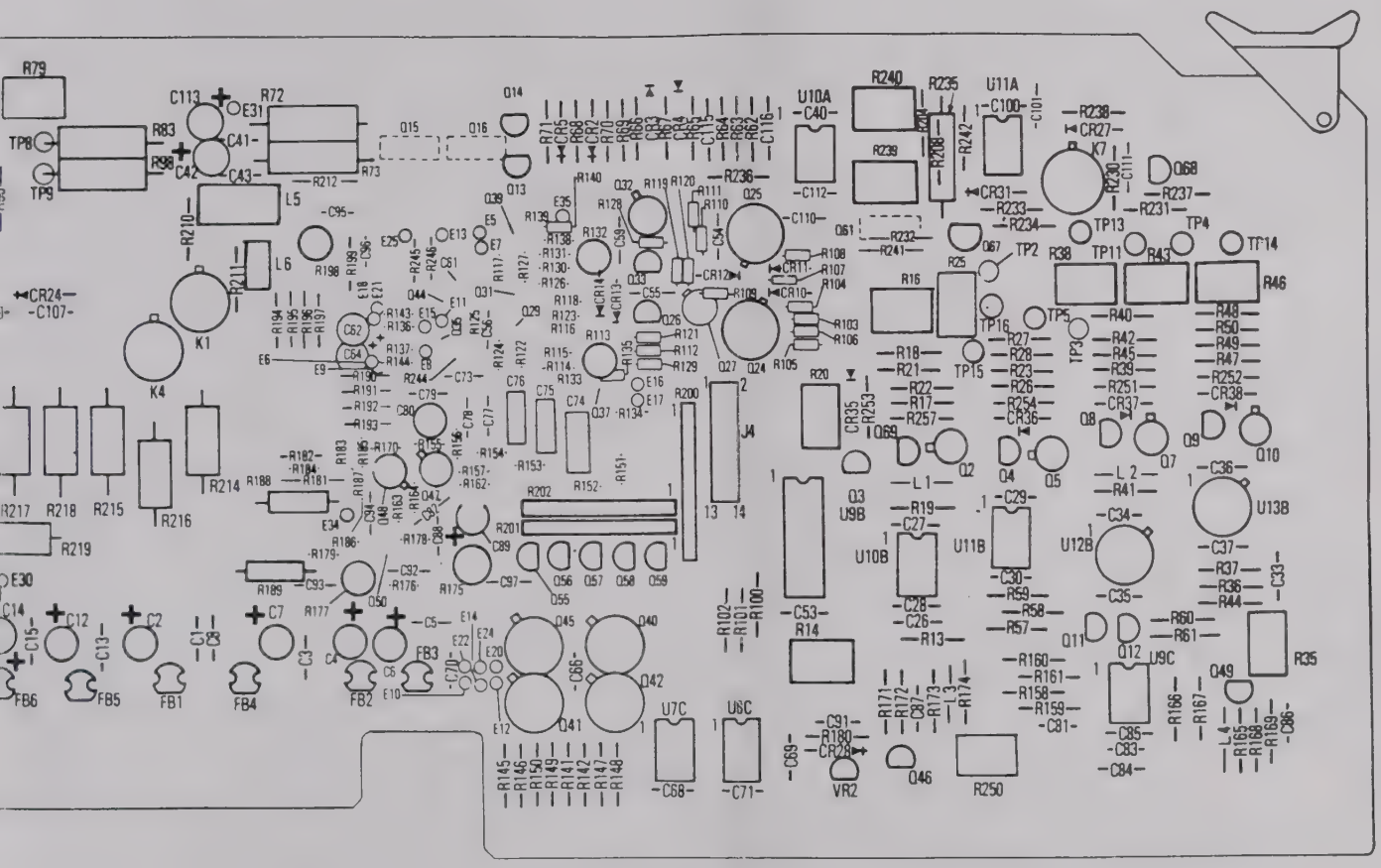


REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 4-17-79	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR		TITLE SCHEMATIC POWER AMPLIFIER BD.	
	RELEASE APPROV R. CONERO 4/8/80			
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030			
	DO NOT SCALE DWG		MODEL NO 859	DWG NO 0103-00-0698 REV Y
	SCALE		CODE IDENT 23338	SHEET 5 OF 5

0103-00-0698

CONTAINS PROPRIETARY INFOR-
RIGHTS BELONGING TO
MAY NOT BE REPRODUCED FOR ANY
CALIBRATION, OPERATION, AND
WITHOUT WRITTEN AUTHORIZATION





MADE FROM 0100-00-0698-3H

WAVETEK		
OUTPUT AMPL		
859	1100-00-0698	F
	SHEET 1 OF 1	

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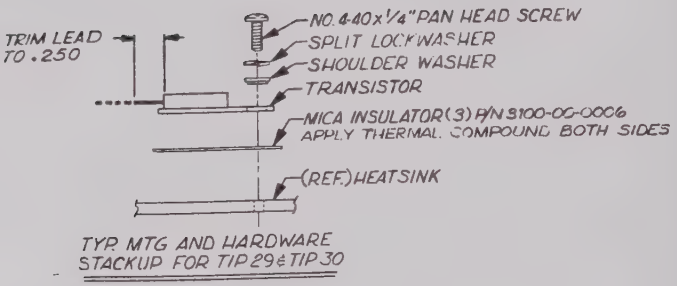
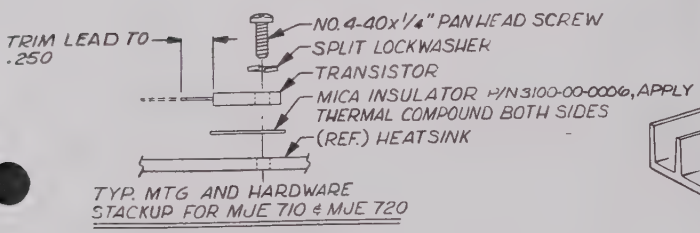
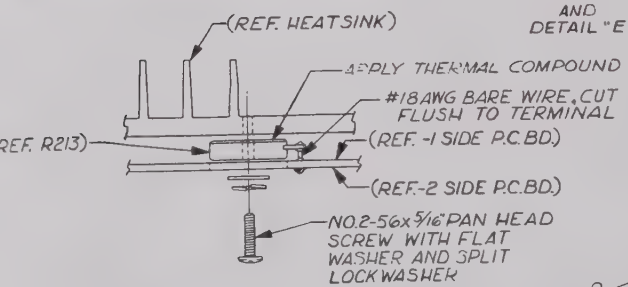


TYP. MTG AND HARDWARE STACKUP FOR TIP29 & TIP30



TYP. MTG AND HARDWARE STACKUP FOR MJE 710 & MJE 720



DETAIL "A"

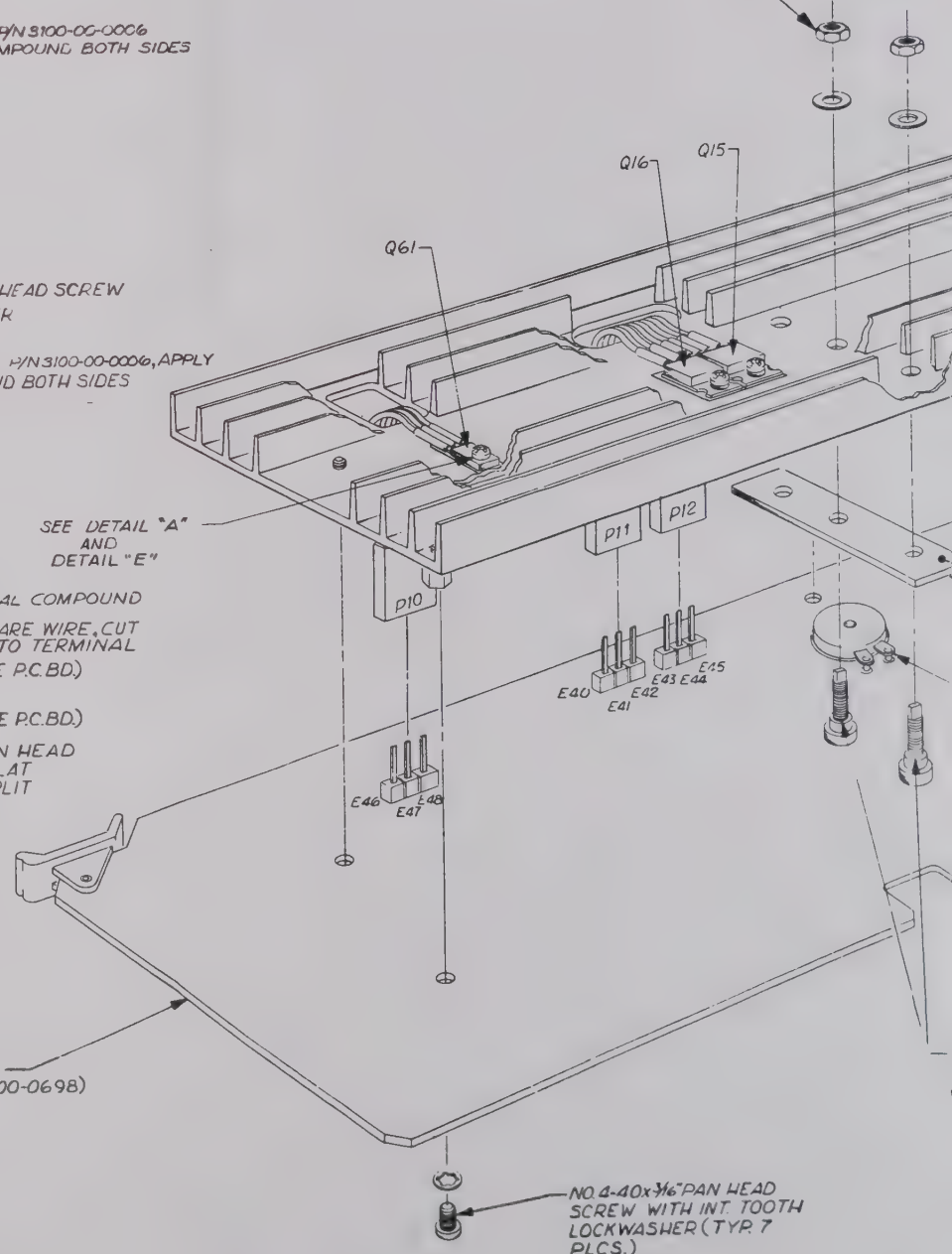
RESISTOR TO HEATSINK MTG.

NO.8-32 HEX NUT WITH FLAT WASHER, THEN APPLY "TORQUE SEAL F-900" (VIOLET) AFTER FINAL CALIBRATION. (TYP. 2 PLCS.)

CAUTION

OVERTIGHTENING OF THESE NUTS WILL BREAK TRANSISTOR STUDS. HOLD FLAT ON STUD WHILE TIGHTENING.

SEE DETAIL "A" AND DETAIL "E"

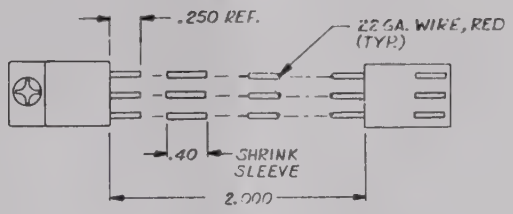


PC BOARD (P/N 0100-00-0698)

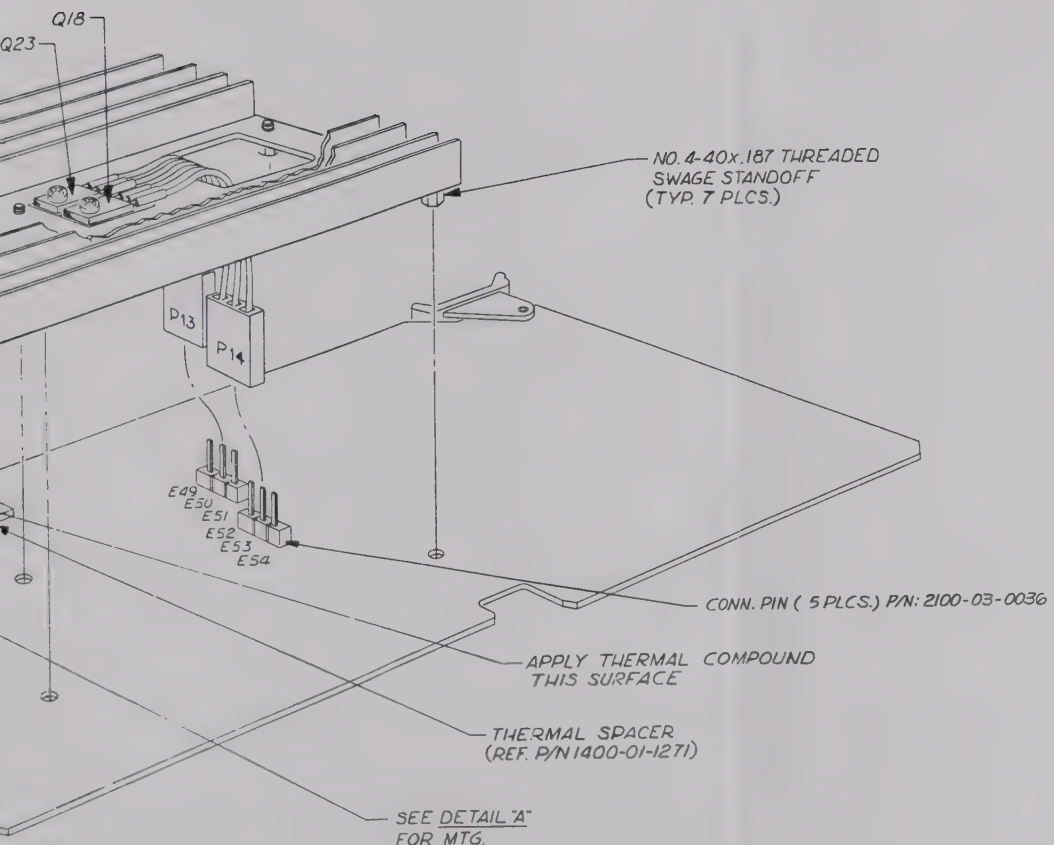
NO.4-40x3/16" PAN HEAD SCREW WITH INT. TOOTH LOCKWASHER (TYP. 7 PLCS.)

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP



DETAIL "E"
WIRE PREP FOR: Q61, Q15, Q16, Q18, & Q23



APPLY THERMAL COMPOUND AROUND SAME ... (TYP 2 PL ...)

CONN. WIRING DESTINATION LISTS

P10

FROM PIN#	TO
1	E46
2	E48
3	E47

P11

FROM PIN#	TO
1	E42
2	E41
3	E40

P12

FROM PIN #	TO
1	E45
2	E44
3	E43

P13

FROM PIN #	TO
1	E51
2	E49
3	E50

P14

FROM PIN #	TO
1	E54
2	E52
3	E53

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 12-17-79	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: ASSEMBLY OUTPUT AMPLIFIER BD (HEATSINK)
	RELEASE APPROV R. CONERO 4/8/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 0101-00-0698 REV AC
	SCALE	CODE IDENT 23338	SHEET 5 OF 5

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, OUTPUT AMP	0101-00-0698	WVTK	0101-00-0698	1
NONE	SCHEMATIC, OUTPUT AMP	0103-00-0698	WVTK	0103-00-0698	1
L6 L8	COIL, 34 MICROH	859-0038	WVTK	1204-00-0038	2
NONE	HEATSINK, OUTPUT AMPL REF: 3200-06-0015	859-9581	WVTK	1400-00-9581	1
NONE	SPACER	859-1271	WVTK	1400-01-1271	1
C36 C93	CAP, CER, 5PF, 1KV	DD-050	CRL	1500-00-5011	2
C77 C79	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	2
C66 C70	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	2
C114 C88	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	2
C82	CAP, CER, MIN, .01MF, 50V	GE50-103ZA	MURAT	1500-01-0310	1
C1 C100 C101 C105 C106 C107 C108 C109 C11 C111 C112 C117 C118 C13 C15 C19 C20 C22 C23 C24 C25 C26 C27 C28 C29 C3 C30 C31 C32 C33 C34 C35 C36 C37 C38 C40 C41 C43 C44 C45 C46 C47 C48 C49 C5 C50 C51 C52 C53 C54 C55 C59 C68 C69 C71 C8 C84 C85 C86 C87 C9 C91 C92 C94 C97	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	65
C73	CAP, CER, 15PF, 1KV	DD-150	CRL	1500-01-5011	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, OUTPUT AMPL	1100-00-0698	AC

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION
	20%
NONE	OUTPUT AMPL
L5 L7	CHOKE, 63 MILLI HENR
L1 L2 L3 L4	CHOKE, 68 MICRO HENR
NONE	SKT, IC, 16PIN
NONE	SKT, IC, 24PIN
NONE	3 POS HEADER
NONE	SPRING SOCKET
P10 P11 P12 P13 P14	HOUSING, CONN 3-POS
NONE	BUSS BAR STANDOFF
NONE	PINS, CONN
J3 J4	HEADER, 14 PIN, 2X7
J2	CONN
NONE	STANDOFF, MALE/FEMAL .187 H, .250 HEX, 4-4
NONE	PC BD EJECTOR
NONE	TRANSIPAD

WAVETEK PARTS LIST	TITLE
	PCA, OUTPUT AMPL

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C103 C110 C95T	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	3
C96	CAP, CER, .0022, 1KV	DD-222SLL	CRL	1500-02-2201	1
C115	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C116	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	1
C91 C83	CAP, MICA, 330PF, 500V	DM15-331J	ARCO	1500-13-3100	2
C78	CAP, MICA, 620PF, 300V 1%	CD15-621F	CDE	1500-16-2100	1
C76	CAP, POLYCARB, .0068MF 50VREF 1509-80-0009	C5R682F	ELPAC	1500-46-8203	1
C75	CAP, POLYCARB, .068MF 50VREF 1509-80-0009	C5R683F	ELPAC	1500-46-8303	1
C74	CAP, POLYCARB, .68MF 50VREF 1509-80-0009	C5R684F	ELPAC	1500-46-8403	1
C80	CAP, VAR, 3-18PF	GKU18000	SPRAG	1500-51-8010	1
C62 C64 C89	CAP, TANT, 2.2MF, 25V	196D225X9025HA1	SPRAG	1500-72-2502	3
C12 C14 C2 C21 C4 C6 C7	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	7
C10 C113 C42	CAP, TANT, 6.8MF, 50V	TAP86.8M50	ITT	1500-76-8503	3
C16 C17 C18 C57 C58 C60 C61 C63 C65 C90	SMD, CAP, CHIP (MARKED RED A) 1MF/50V BX	ULA555E104MIT60	AVX	1509-90-0017	10

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, OUTPUT AMPL	1100-00-0698	AC

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	HEATSINK, PRESS ON, TO-5
	WASHER
FB1 FB2 FB3 FB4 FB5 FB6	BALUN CORE
NONE	INSULATOR, MICA
K1 K2 K4 K5 K6 K7	RELAY
R113 R132	POT, TRIM, 100
R175	POT, TRIM, 50
R177 R198	POT, TRIM, 500
R84	POT, TRIM, 20T, 100K
R38	POT, TRIM, 20T, 10K
R16 R79 R95	POT, TRIM, 20T, 20K
R54	POT, TRIM, 20T, 2K
R14 R239 R240 R35 R74	POT, TRIM, 20T, 1K
R20 R25 R43 R46	POT, TRIM, 20T, 200
R250	POT, 20T, TOP TRIM, 2MEG
R76 R87	POT, 20T, TOP TRIM,

WAVETEK PARTS LIST	TITLE
	PCA, OUTPUT AMPL

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	859-0698	WVTK	1700-00-0698	1
Y	EC15HL34	MCEL	1800-00-0017	2
Y	IR-2	DALE	1800-00-0018	4
	16-DIP	CINCH	2100-03-0022	2
	DILB-24P-108	BURND	2100-03-0029	2
	87348-3	AMP	2100-03-0036	5
	6-330808-5	AMP	2100-03-0037	8
	87499-5	AMP	2100-03-0042	5
	2110-001	ARTWR	2100-05-0024	14
	87667-2	AMP	2100-05-0030	15
	CA-D14RSP100-230-090	CA	2100-05-0053	2
	27-848	AMPH	2100-07-0011	1
E 0	1425-M12-F05A-440	UNICP	2800-02-0030	7
	103 ORANGE	CALMK	2800-07-0011	2
	10123N	METRS	2800-11-0003	13

	REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
		500 OHM				
	R110	RES. CAR. 1/8W. 5%. 22	RC05GF220J	AB	4700-05-0220	1
	R103 R108 R116 R117 R118 R122 R123 R126 R127 R133 R135 R136 R137 R138 R140 R143 R144 R136 R179 R182 R184	RES. CAR. 1/8W. 5%. 33	RC05GF330J	AB	4700-05-0330	21
	R109 R112 R115 R119 R121 R124 R125 R128 R130 R178 R183 R185	RES. CAR. 1/8W. 5%. 51	RC05GF510J	AB	4700-05-0510	12
	R164	RES. CAR. 1/8W. 5%. 100	RC05GF101J	AB	4700-05-1000	1
	R114 R131	RES. MF. 1/8W. 5%. 1K	RC05GF102J	AB	4700-05-1001	2
	R157 R162 R163 R170	RES. CAR. 1/8W. 5%. 100K	RC05GF104J	AB	4700-05-1003	4
	R243 R244 R245 R246	RES. CAR. 1/8W. 5%. 20	RC05GF200J	AB	4700-05-2009	4
	R151 R152 R153 R154 R155	RES. CAR. 1/8W. 5%. 22M	RC05GF226J	AB	4700-05-2205	5
	R111 R120 R129	RES. CAR. 1/8W. 5%. 270	RC05GF271J	AB	4700-05-2700	3
	R134	RES. CAR. 1/8W. 5%. 390	RC05GF391J	AB	4700-05-3900	1
	R105 R106 R139	RES. CAR. 1/8W. 5%. 470	RC05GF471J	AB	4700-05-4700	3
	R104 R107 R176 R186	RES. CAR. 1/8W. 5%. 4 7K	RC05GF472J	AB	4700-05-4701	4
	R188 R189	RES. C. 1/2W. 5%. 620	RC-1/2-621J	STKPL	4700-25-6200	2

ASSEMBLY NO.	REV
1100-00-0698	AC

PAGE 3

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA. OUTPUT AMPL	1100-00-0698	AC

PAGE 5

	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	2225B	THERM	2800-11-0014	1
	851547F015	MOT	2800-11-0015	3
	2873000902	FARIT	3100-00-0002	6
	64-21-023-106	ASHVL	3100-00-0006	3
	CSW-5	HI-G	4500-00-0016	6
	3329H-1-101	BOURN	4600-01-0100	2
	3329H-1-500	BOURN	4600-05-0001	1
	3329H-1-501	BOURN	4600-05-0108	2
	68WR100K	BECK	4609-90-0001	1
	68WR10K	BECK	4609-90-0002	1
	68WR20K	BECK	4609-90-0003	3
	68WR2K	BECK	4609-90-0004	1
	68WR1K	BECK	4609-90-0005	3
	68WR200	BECK	4609-90-0020	4
	68WR2M	BECK	4609-90-0022	1
	68WR500	BECK	4609-90-0023	2

	REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	R11 R238 R251 R252 R33 R65	RES. MF. 1/8W. 1%. 100	RN55D-1000F	TRW	4701-03-1000	6
	R148 R149 R165 R17 R171 R174 R19 R256 R257 R26 R41 R58 R59 R60 R61 R68 R71 R89 R91 R93	RES. MF. 1/8W. 1%. 1K	RN55D-1001F	TRW	4701-03-1001	20
	R230 R51 R53	RES. MF. 1/8W. 1%. 10K	RN55D-1002F	TRW	4701-03-1002	3
	R22 R23 R255 R45 R49	RES. MF. 1/8W. 1%. 100K	RN55D-1003F	TRW	4701-03-1003	5
	R227	RES. MF. 1/8W. 1%. 1.21K	RN55D-1211F	TRW	4701-03-1211	1
	R180	RES. MF. 1/8W. 1%. 124	RN55D-1240F	TRW	4701-03-1240	1
	R167	RES. MF. 1/8W. 1%. 140	RN55D-1400F	TRW	4701-03-1400	1
	R12 R181 R187 R241 R34	RES. MF. 1/8W. 1%. 1 5K	RN55D-1501F	TRW	4701-03-1501	5
	R13	RES. MF. 1/8W. 1%. 1 62K	RN55D-1621F	TRW	4701-03-1621	1
	R210 R225 R236 R88	RES. MF. 1/8W. 1%. 1 78K	RN55D-1781F	TRW	4701-03-1781	4
	R69 R70	RES. MF. 1/8W. 1%. 182	RN55D-1820F	TRW	4701-03-1820	2
	R36	RES. MF 1/8W. 1%. 1 96K	RN55D-1961F	TRW	4701-03-1961	1
	R21 R28 R42 R50	RES. MF. 1/8W. 1%. 200	RN55D-2000F	TRW	4701-03-2000	4
	R166 R18 R242 R27 R40 R48 R56 R81 R96	RES. MF. 1/8W. 1%. 2K	RN55D-2001F	TRW	4701-03-2001	9

ASSEMBLY NO.	REV
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WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA. OUTPUT AMPL	1100-00-0698	AC

PAGE 6

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE

PARTS LIST
PCA. OUTPUT AMPL.

MODEL NO	DWG NO	
859	1100-00-0698	AC
CAGE IDENT 23338	SHEET 1 OF 2	

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/P*
R231	RES, MF, 1/8W, 1%, 21.5K	RN55D-2152F	TRW	4701-03-2152	1
R169	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R1 R172 R211T R3	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	4
R99	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R173	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	1
R199 R253 R254	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R168	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	1
R204	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	1
R10	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	1
R63	RES, MF, 1/8W, 1%, 38.3K	RN55D-3832F	TRW	4701-03-3832	1
R228T	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R190 R191 R192 R193 R194 R195 R196 R197 R233 R234	RES, MF, 1/8W, 1%, 39.2	RN55D-39R2F	TRW	4701-03-3929	10
R75	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	1
R9 R90 R92	RES, MF, 1/8W, 1%, 46.4K	RN55D-4642F	TRW	4701-03-4642	3
R64	RES, MF, 1/8W, 1%, 47.5K	RN55D-4752F	TRW	4701-03-4752	1
R208 R31 R32 R80	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	4

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, OUTPUT AMPL	1100-00-0698	AC

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MF
R214 R215 R217	RES, MF, 2W, 1%, 16.67	MS223-1
R221 R224	RES, MF, 3W, 1%, 20.83	MS223-2
R216 R218	RES, MF, 3W, 1%, 66.67	MS223-6
R219	RES, MF, 2W, 1%, 50	MS245-5
R220 R222 R223	RES, MF, 6W, 1%, 33.33	MS260-3
R158 R159 R160 R161	RES, MF, 1/4W, 1%, 10M	CC1005F
CR35 CR36 CR37 CR38	DIODE	1N746A
CR31 CR6	DIODE	1N751A
CR12 CR28	DIODE	1N4740A
CR32 CR33 CR7 CR9	DIODE	1N5282
CR2 CR22 CR23 CR24 CR25 CR26 CR27 CR3 CR4 CR5	DIODE	1N4148
CR1 CR10 CR11 CR8	DIODE	5082-28
CR13 CR14	DIODE, M/PR, 1N4740A QTY: 2: 4801-01-4740	4898-00
CR17 CR18 CR19 CR20 CR21	DIODE PACK	MMD7000
Q41 Q45	TRANS	2N2219A

WAVETEK PARTS LIST	TITLE
	PCA, OUTPUT AMPL

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/P*
R141 R142 R145 R146 R212 R226 R37 R39 R44 R47 R52 R57 R6 R66 R67 R7 R8	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	17
R85	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	1
R232 R82 R97	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	3
R147 R150 R55	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	3
R77	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	1
R86	RES, MF, 1/8W, 1%, 7.87K	RN55D-7871F	TRW	4701-03-7871	1
R100 R101 R102	RES, MF, 1/8W, 1%, 78.7	RN55D-78R7F	TRW	4701-03-7879	3
R237	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	1
R62	RES, MF, 1/8W, 1%, 95.3K	RN55D-9532F	TRW	4701-03-9532	1
R235 R72 R73 R83 R98	RES, WW, 3W, 3%, 5	CW-2B	DALE	4702-57-5009	5
R2 R3	RES MODULE	4116R-001-102	BOURN	4770-00-0019	2
R4	RES MODULE	4310R-101-102	BOURN	4770-00-0022	1
R202	RES MODULE	4310R102-471	BOURN	4770-00-0027	1
R200 R229	RES MODULE	4310R102-472	BOURN	4770-00-0028	2
R201	RES MODULE, 47K	4310R-101-473	BOURN	4770-00-0030	1
R213	RES, CAR, 15W, 1%, 50	MP312-50	CADDO	4799-00-0050	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, OUTPUT AMPL	1100-00-0698	AC

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MF
Q27 Q32	TRANS	2N2369A
Q40 Q42	TRANS	2N2905A
Q11 Q22	TRANS	2N3565
Q8 Q9	TRANS	2N3642
Q13 Q49 Q62 Q63 Q64 Q66 Q68	TRANS	2N3904
Q14 Q46 Q55 Q56 Q57 Q58 Q59 Q65 Q69	TRANS	2N3906
Q17 Q3 Q4 Q67	TRANS	2N4122
Q12	TRANS	2N4248
Q6	TRANS	2N5462
Q1 Q19 Q20 Q21	TRANS	2N5485
Q26 Q33	TRANS	MPS-L08
Q16	TRANS	TIP-29
Q15	TRANS	TIP-30
Q52	TRANS	BFR94
Q10 Q7	TRANS	SD215DE
Q53	TRANSISTOR	MRF331

WAVETEK PARTS LIST	TITLE
	PCA, OUTPUT AMPL

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

FOR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
16, 67	CADDO	4799-00-0051	3
20, 83	CADDO	4799-00-0052	2
66, 67	CADDO	4799-00-0053	2
50	CADDO	4799-00-0054	1
33, 33	CADDO	4799-00-0055	3
	AB	4799-00-0056	4
	FAIR	4801-01-0746	4
	FAIR	4801-01-0751	2
	MOT	4801-01-4740	2
	FAIR	4801-01-5282	4
	FAIR	4807-02-6666	10
311	HP	4809-02-2811	4
-0016	WVTK	4898-00-0016	1
	MOT	4899-00-0025	5
	NSC	4901-02-2191	2

ASSEMBLY NO.	REV
1100-00-0698	AC

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
Q2 Q5	TRANS	MEM511	SILX	4902-00-5111	2
Q18 Q61	TRANS	MJE710	MOT	4902-00-7100	2
Q23	TRANS	MJE720	MOT	4902-00-7200	1
Q24 Q25	TRANS	4902-02-5730	WVTK	4902-02-5730	2
Q38 Q39	SMD, TRANS, MMT 3960	MMT3960	MOT	4902-03-9600	2
Q30 Q31 Q51	SMD, TRANS, MMT 3960 A	MMT3960A	MOT	4902-03-9601	3
Q28 Q29 Q36 Q37 Q50	SMD, TRANS, MMT 4261	MMT4261	MOT	4902-04-2610	5
Q35 Q44	TRANS, M/PR, MMT3960 QTY: 2: 4902-03-9600	4998-00-0046	WVTK	4998-00-0046	1
Q34 Q43	TRANS, M/PR, MMT4261 QTY: 2: 4902-04-2610	4998-00-0047	WVTK	4998-00-0047	1
Q47 Q48	TRANS, M/PR QTY: 2: 4902-00-2030	4998-00-0048	WVTK	4998-00-0048	1
	WIRE, HU, 22GA	H0101029 (WHT)	JUDD	6000-32-2009	.6
NONE	CABLE, COAX, 75 OHM	9221	BELDN	6001-40-0006	1
NONE	ASSY, RIBBON CABLE	6002-00-0012	WVTK	6002-00-0012	1
U2C U5C U6C	IC	MLM339P	MOT	7000-03-3900	3
U5A	IC	LM348N	NSC	7000-03-4800	1

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA, OUTPUT AMPL	1100-00-0698	AC

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GR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	MOT	4901-02-3691	2
	NSC	4901-02-9051	2
	FAIR	4901-03-5650	2
	FAIR	4901-03-6420	2
	FAIR	4901-03-9040	7
	FAIR	4901-03-9060	9
	NSC	4901-04-1220	4
	FAIR	4901-04-2480	1
	MOT	4901-05-4620	1
	MOT	4901-05-4850	4
	FAIR	4902-00-0080	2
	TI	4902-00-0290	1
	TI	4902-00-0300	1
	AMPRX	4902-00-0940	1
	SIG	4902-00-2140	2
		4902-00-3310	1

ASSEMBLY NO.	REV
1100-00-0698	AC

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U6A	IC	LF353N	NSC	7000-03-5300	1
U10A U10B U11A U11B U7C U8A U8C U9A U9C	OP-AMP	LF356N	NSC	7000-03-5600	9
U1A U2A	IC	AD565JD	ANDEV	7000-05-6500	2
U12B U13B	IC	CA3140S	RCA	7000-31-4001	2
U7A	IC	CD4053BE	RCA	7000-40-5300	1
U3A U4A	IC	AD7533LN	ANDEV	7000-75-3300	2
U1C U4C	CMOS, DCDR, DUAL 1-4	F4555B	FAIR	8000-45-5500	2
U3C	TTL, NAND, QUAD 2INP	74LS03	TI	8000-74-0310	1
VR1	VOLT REG	UA78M05HC	FAIR	8000-78-0501	1
VR2	VOLT REG	78L82	FAIR	8000-78-8210	1
U9B	ECL, XOR/XNOR, TRI2INP	MC10107	MOT	8001-01-0700	1
U8B	CMOS, D-F/F, HEX	74C174	NAT	8007-41-7430	1
U1B U2B U3B U4B U5B U6B U7B	CMOS, D-F/F, OCT	74C374	NAT	8007-43-7430	7

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA, OUTPUT AMPL	1100-00-0698	AC

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REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, OUPUT AMPL.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO: 859 / DWG NO: 1100-00-0698 / REV: AC
	SCALE		CODE IDENT: 23338 / SHEET 2 OF 2

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NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PIGGY BACK MODULE	859-1133	WVTK	1700-00-1133	1
R1	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1
Q1	TRANS	2N3906	FAIR	4901-03-9060	1
Q2	TRANS	MEM511	SILX	4902-00-5111	1

WAVETEK PARTS LIST

TITLE: PCA, MODULE, PIGGY BACK, (MEM511)

ASSEMBLY NO. 1208-00-1133

REV

PAGE 1

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH WAVETEK PROCESS

DRAWN | DATE

PROJENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

PARTS LIST
PCA, MODULE, PIGGY BACK
(MEM 511)

MODEL NO 859 | DWG NO 1208-00-1133 | REV

CODE IDENT 23338 | SHEET 1 OF 2

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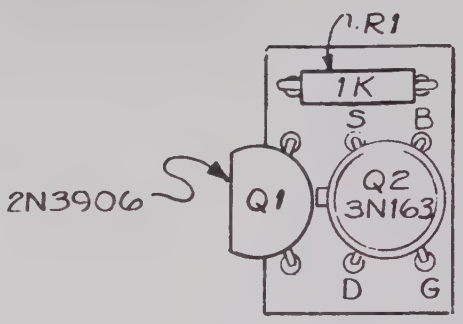
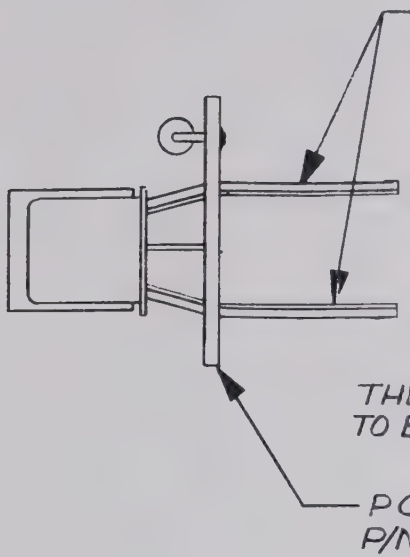
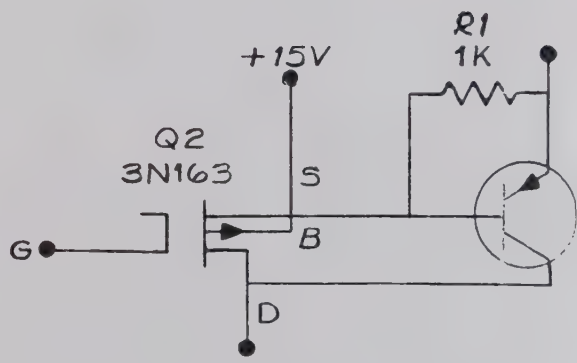




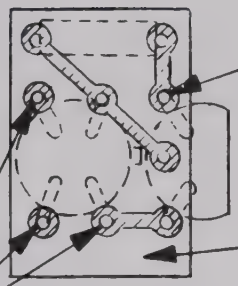


NOTE: UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-4829

REV	ECN	BY	DATE	APP
A	# 3990	C	10/17/83	

STOCK LEAD
LENGTH (4 PLCS)



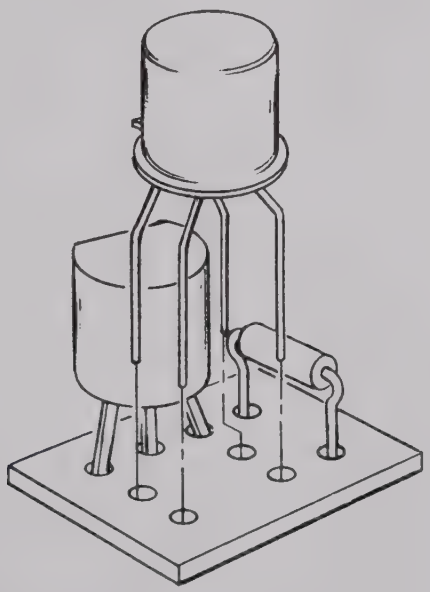
THIS LEAD TO BE
LEFT LONG

CIRCUIT SIDE PC BOARD

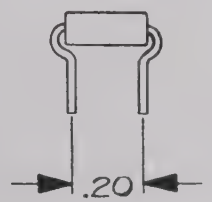
ESE LEADS ARE
BE LEFT LONG

BOARD
1700-00-1133

Q1
2N3906



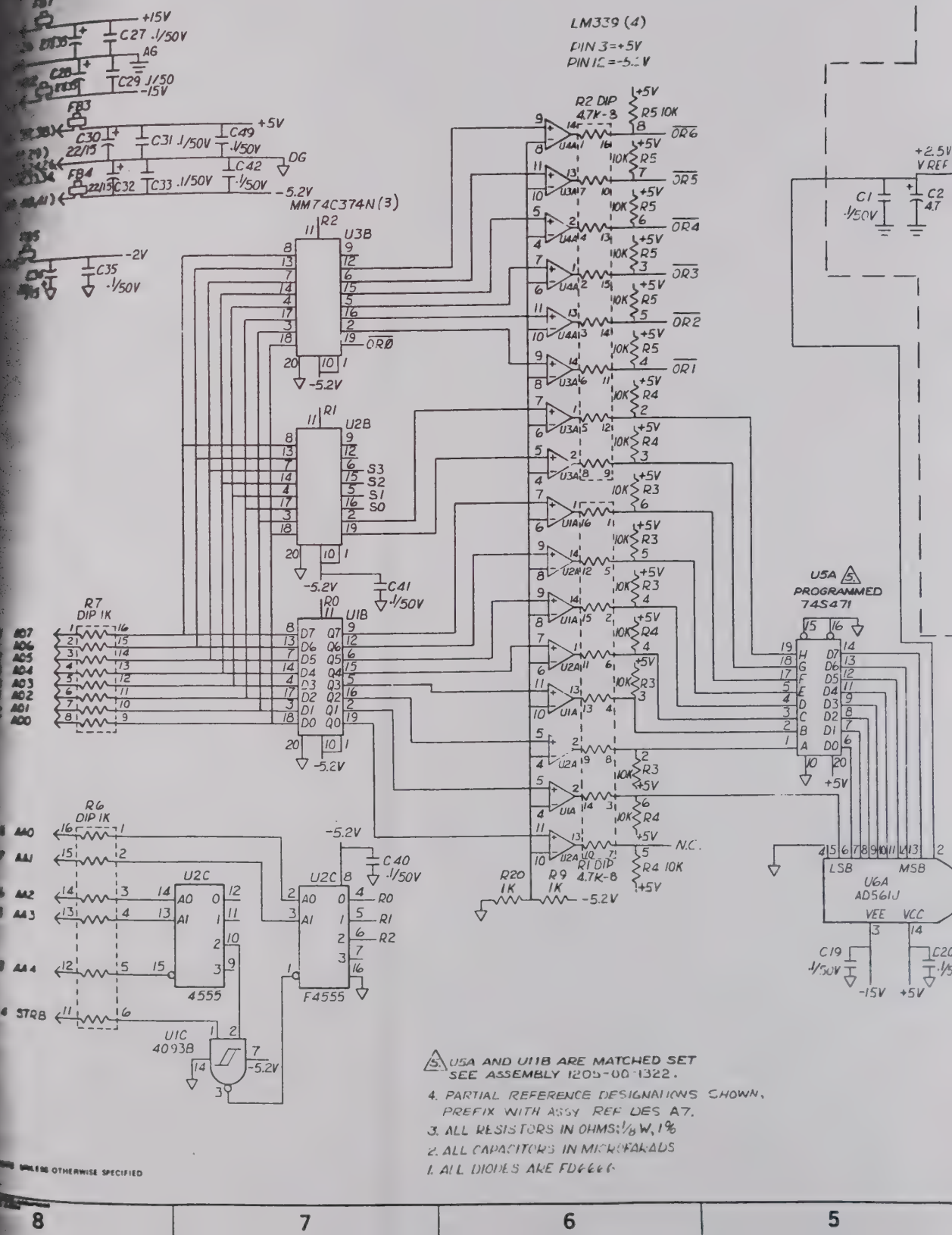
COMPONENT LEAD
LOCATIONS



PREP "R1" LEADS
AS SHOWN

EMOVE ALL BURRS ND BREAK SHARP EDGES	DRAWN: CHERMACK	DATE: 5-11-83	WAVETEK SAN DIEGO • CALIFORNIA
TERIAL	PROJ ENGR		TITLE: ASSEMBLY MODULE, PIGGY BACK
	RELEASE APPROV		
ISH VETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 859	DWG NO. 1208-00-1133 / REV A
	SCALE: NONE	CODE IDENT 23338	SHEET 2 OF 2

...CONTAINS PROPRIETARY INFOR-
...RIGHTS BELONGING TO
...MAY NOT BE REPRODUCED FOR ANY
...CALIBRATION, OPERATION, AND
...WITHOUT WRITTEN AUTHORIZATION.



5. U5A AND U11B ARE MATCHED SET SEE ASSEMBLY 1205-00-1322.

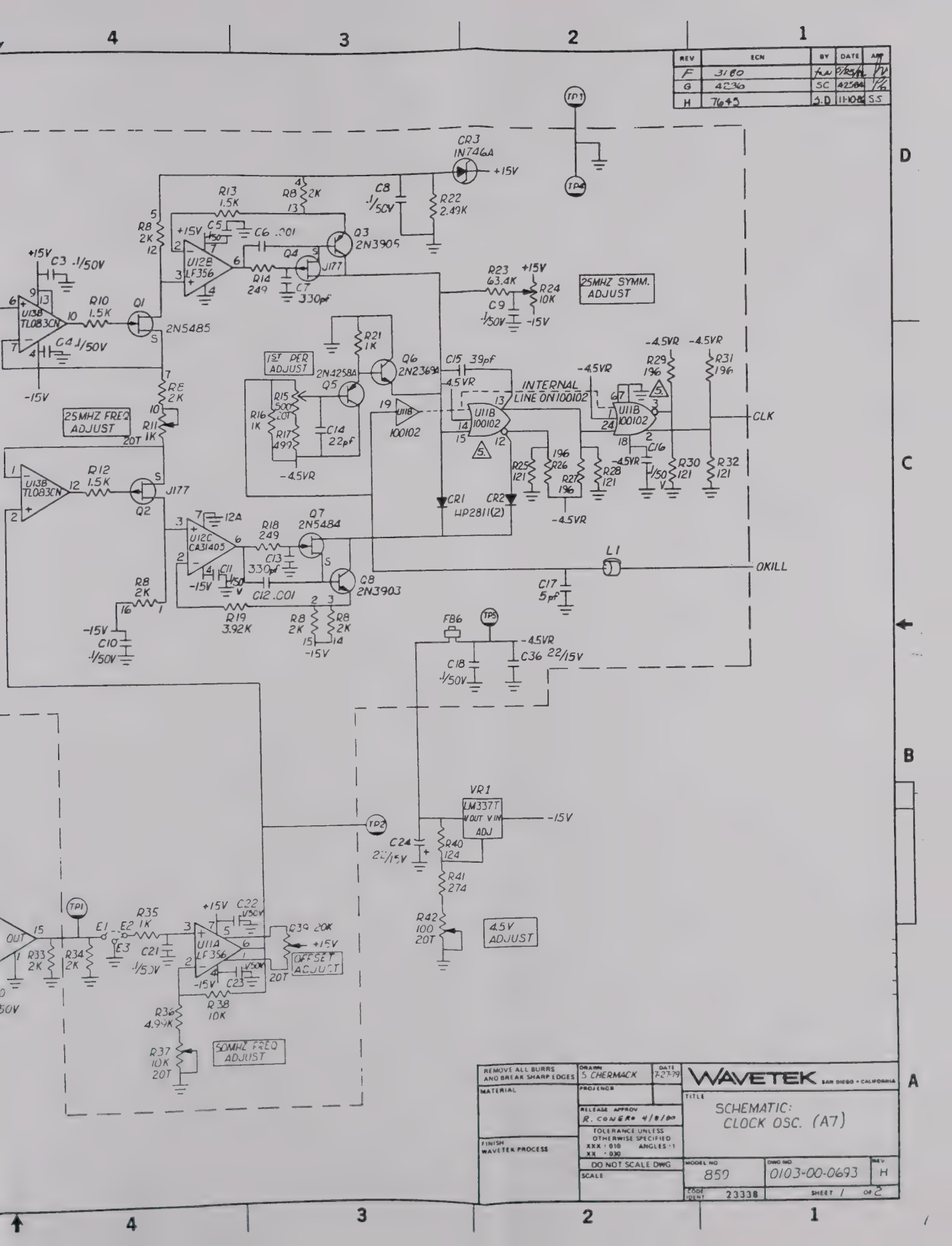
4. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSY REF DES A7.

3. ALL RESISTORS IN OHMS: 1/8 W, 1%

2. ALL CAPACITORS IN MICROFARADS

1. ALL DIODES ARE FD6666

...UNLESS OTHERWISE SPECIFIED



REV | ECN | BY | DATE | APP
F | 3180 | | | |
G | 4236 | SC | 4258A | |
H | 7645 | S.D | 11-10-82 | SS
CR3 1N746A
+15V
C8 .1/50V
R22 2.49K
R13 1.5K
R8 2K
C5 .1/50
C6 .001
Q3 2N3905
U12B LF356
Q4 J177
R14 249
C7 330pf
R23 63.4K
R24 10K
C9 .1/50V
-15V
25MHZ SYMM. ADJUST
C3 .1/50V
U13B TL083CN
R10 1.5K
Q1 2N5485
C4 .1/50V
R21 1K
1ST PER ADJUST
Q6 2N2369A
2N4258A Q5
C15 39pf
-4.5VR
INTERNAL LINE ON100102
U11B 100102
R29 196
R31 196
CLK
R15 500 20T
R16 1K
R17 499
C14 22pf
U11B 100102
R25 121
R26 196
R27 196
R28 121
C16 .1/50V
R30 121
R32 121
R8 2K
R11 1K 20T
25MHZ FREQ ADJUST
U13B TL083CN
R12 1.5K
Q2 J177
CR1 CR2 HP2811(2)
U12C CA31405
R18 249
Q7 2N5484
C13 330pf
C11 .1/50V
C12 .001
Q8 2N3903
R19 3.92K
L1
OKILL
C17 5pf
C10 .1/50V
FB6
C18 .1/50V
C36 22/15V
VR1 LM337T
VOUT VIN ADJ
C24 22/15V
R40 124
R41 274
R42 100 20T
4.5V ADJUST
OUT
R33 2K
R34 2K
E1 E2 E3
R35 1K
C21 .1/50V
U11A LF356
C22 .1/50V
C23 .1/50V
R39 20K
OFFSET ADJUST
R36 4.99K
R38 10K
R37 10K 20T
50MHZ FREQ ADJUST
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S CHERMACK
DATE 7-27-79
PROJ ENGR
RELEASE APPROV R. CONERO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC: CLOCK OSC. (A7)
MODEL NO 859
DWG NO 0103-00-0693
REV H
CODE IDENT 23338
SHEET 1 OF 2

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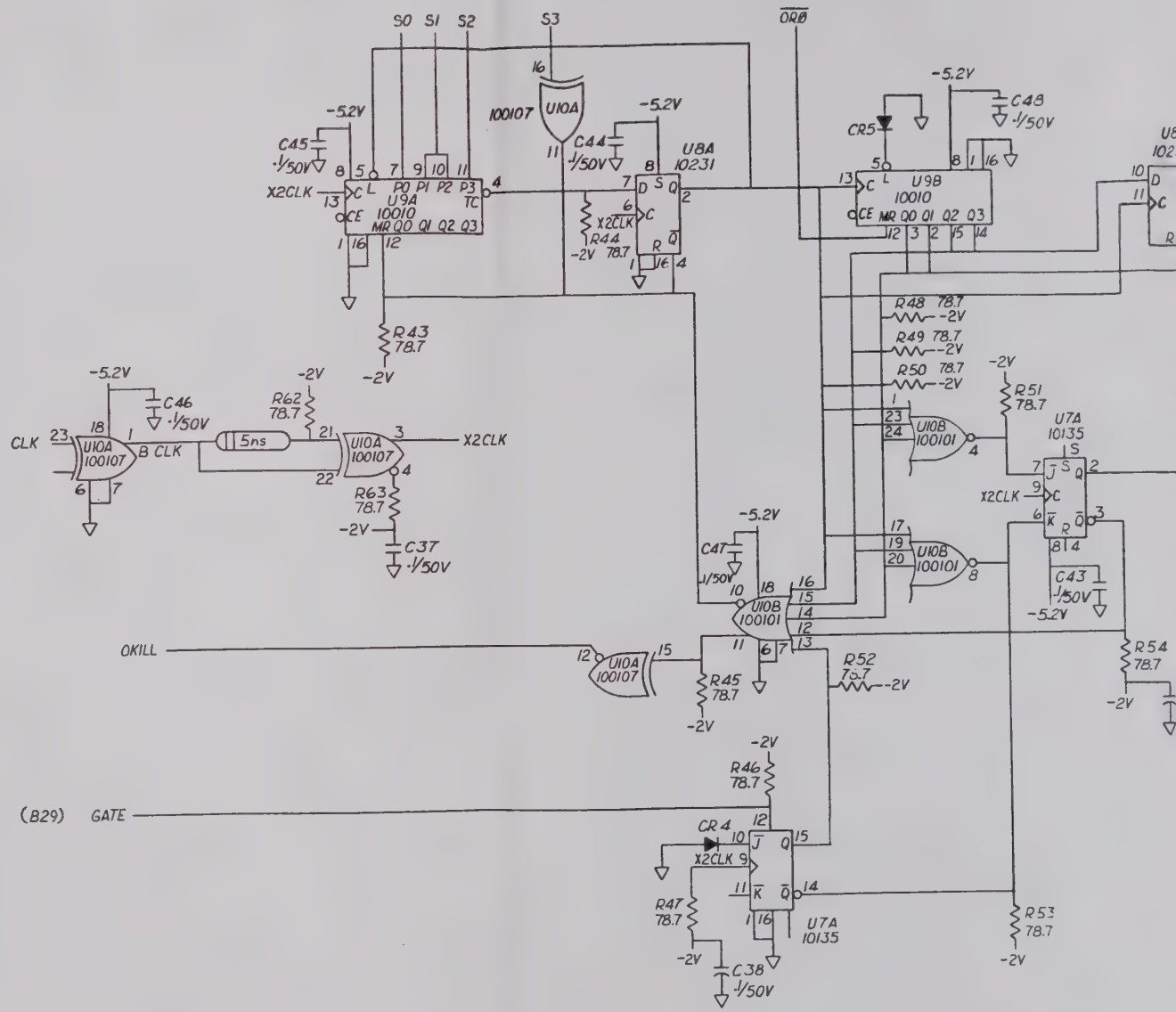

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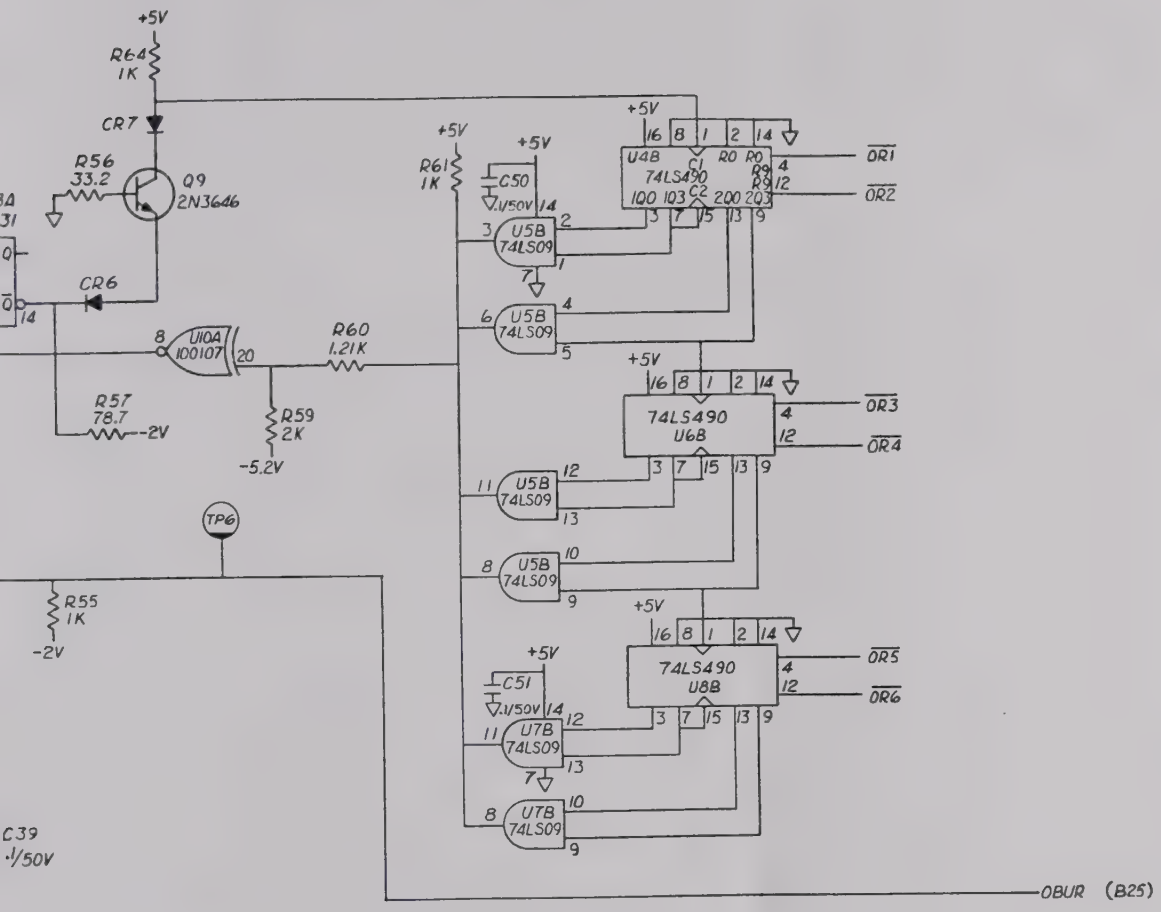

REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN J. CHERMACK	DATE 7-27-79	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ/ENGR		TITLE: SCHEMATIC: CLOCK OSC.
	RELEASE APPROV R CONDRO 9/8/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 859 / DWG NO. 0103-00-0693 / REV H
	SCALE		CODE IDENT 23338 / SHEET 2 OF 2

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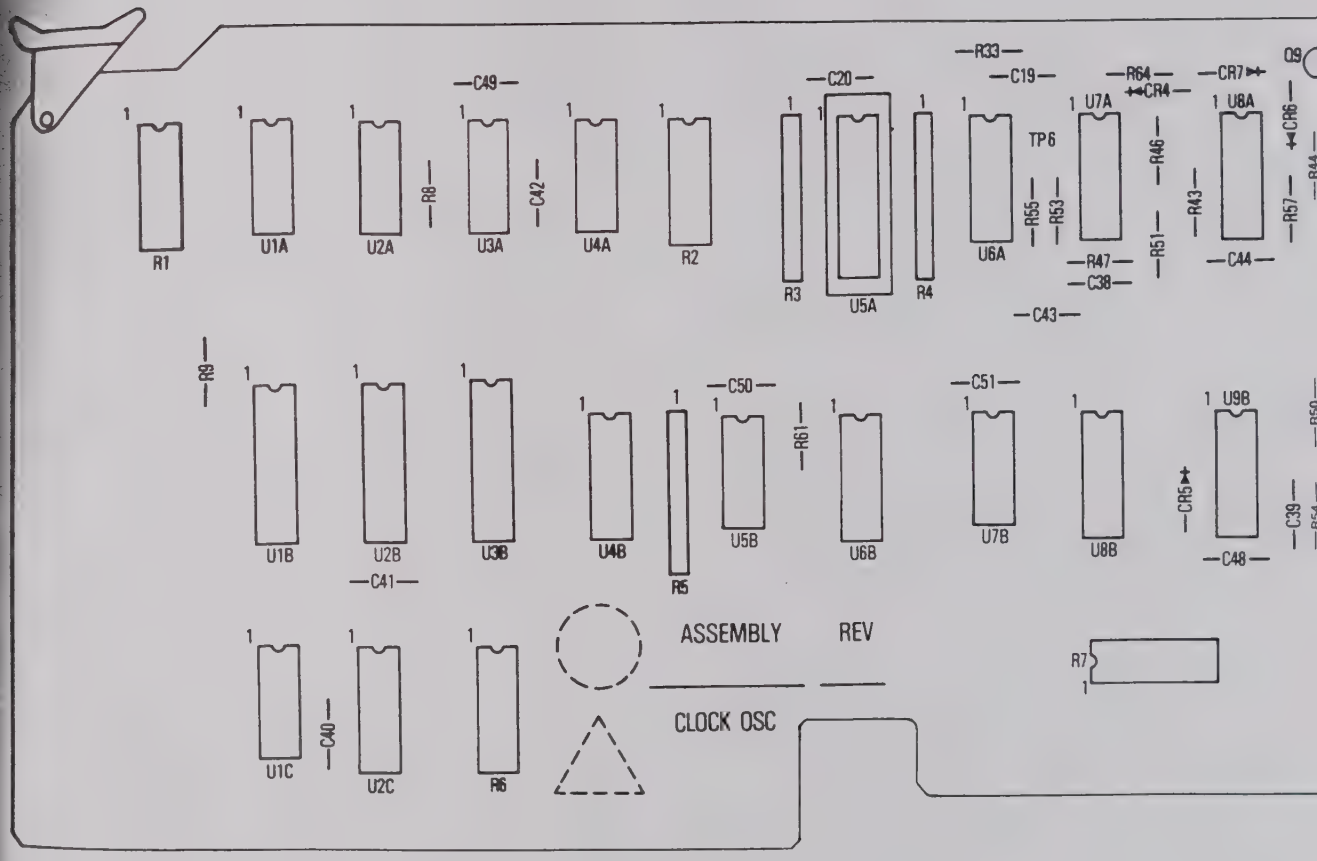

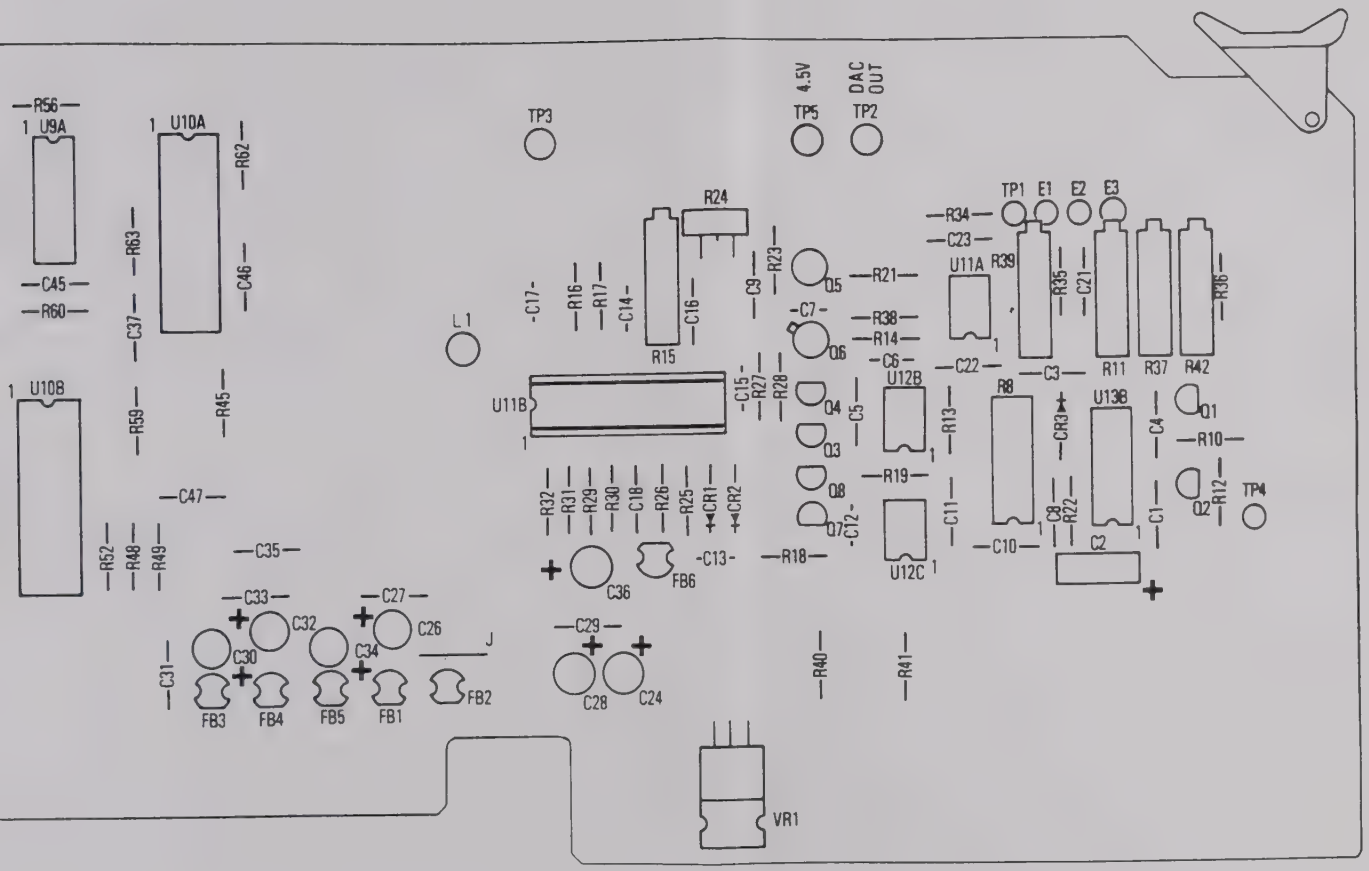

MADE FROM 0100-00-0693-5F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROTOTYPE		TITLE: CLOCK OSCILLATOR
FINISH: WAVETEK PREFERS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX .010 ANGLES ± .XX .030		
	DO NOT SCALE DWG	MODEL NO: 859	DWG NO: 1100-00-0693 REV: F
	SCALE	ORDER NO: 23338	SHEET 1 OF 1

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REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CLOCK OSC	0101-00-0693	WVTK	0101-00-0693	1
NONE	SCHEMATIC, CLOCK OSC	0103-00-0693	WVTK	0103-00-0693	1
L1	INDUCTOR, 60.4MHZ	172-604	WVTK	1204-00-0604	1
NONE	ASSY, SELECTED SET OF IC'S	MOD 859-1322	WVTK	1205-00-1322	1
NONE	PARTITION	859-9481	WVTK	1400-00-9481	2
NONE	PARTITION	859-9491	WVTK	1400-00-9491	1
NONE	PARTITION	859-9501	WVTK	1400-00-9501	1
NONE	POST REF: 3200-02-0004	859-9511	WVTK	1400-00-9511	4
NONE	COVER	859-9523	WVTK	1400-00-9523	1
C17	CAP, CER, 5PF, 1KV	DD-050	CRL	1500-00-5011	1
C12 C6	CAP, CER, .001MF, 1KV	DD-102	CRL	1500-01-0211	2
C1 C10 C11 C16 C18 C19 C20 C21 C22 C23 C27 C29 C3 C31 C33 C35 C37 C38 C39 C4 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C5 C50 C51 C8 C9	CAP, CER, MON., 1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	35
C14	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	1
C13 C7	CAP, CER, 330PF, 1KV	DD-331	CRL	1500-03-3111	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, CLOCK OSC	1100-00-0693	

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-M
R39	POT, TRIM, 20T, 20K	43P203
R15	POT, TRIM, 20T, 500	43P501
R16 R20 R21 R35 R55 R61 R64 R9	RES, MF, 1/8W, 1%, 1K	RN55D-
R36	RES, MF, 1/8W, 1%, 10K	RN55D-
R25 R28 R30 R32	RES, MF, 1/8W, 1%, 121	RN55D-
R60	RES, MF, 1/8W, 1%, 1.21K	RN55D-
R40	RES, MF, 1/8W, 1%, 124	RN55D-
R10 R12 R13	RES, MF, 1/8W, 1%, 1.5K	RN55D-
R33 R34 R59	RES, MF, 1/8W, 1%, 2K	RN55D-
R14 R18	RES, MF, 1/8W, 1%, 249	RN55D-
R22	RES, MF, 1/8W, 1%, 2.49K	RN55D-
R41	RES, MF, 1/8W, 1%, 274	RN55D-
R56	RES, MF, 1/8W, 1%, 33.2	RN55D-
R19	RES, MF, 1/8W, 1%, 3.92K	RN55D-
R17	RES, MF, 1/8, 1%, 499	RN55D-
R36	RES, MF, 1/8W, 1%, 4.99K	RN55D-

WAVETEK PARTS LIST	TITLE
	PCA, CLOCK OSC

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C15	CAP, MICA, 39PF, 500V	DM15-390J	ARCO	1500-13-9000	1
C24 C30 C32 C34 C36	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	5
C26 C28	CAP, TANT, 27MF, 35V	196D276X0035TE4	SPRAG	1500-72-7602	2
C2	CAP, TANT, 4.7MF, 35V	150D475X9035B2	SPRAG	1500-74-7502	1
NONE	CLOCK	859-0693	WVTK	1700-00-0693	1
NONE	SOCKET, 20 PIN	DIBL-20P-108	BURND	2100-03-0051	1
NONE	SOCKET, SINGLE IN-LINE, 12 PIN	C47S12-A	TI	2100-03-0073	2
TP1 TP2 TP3 TP4 TP5 TP6	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	6
NONE	PC BD EJECTOR	103 YELLOW	CALMK	2800-07-0012	2
NONE	JUMPER	461-2871-01-03-10	CAMB	3000-00-0034	1
NONE	PINS, JUMPER	450-3704-01-03	CAMB	3000-00-0035	3
FB1 FB2 FB3 FB4 FB5 FB6	BALUN CORE	2873000902	FARIT	3100-00-0002	6
R24	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	1
R42	POT, TRIM, 20T, 100	43P101	SPECT	4600-11-0100	1
R11	POT, TRIM, 20T, 1K	43P102	SPECT	4600-11-0202	1
R37	POT, TRIM, 20T, 10K	43P103	SPECT	4600-11-0301	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, CLOCK OSC	1100-00-0693	

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-
R23	RES, MF, 1/8W, 1%, 63.4K	RN55D
R43 R44 R45 R46 R47 R48 R49 R50 R51 R52 R53 R54 R57 R62 R63	RES, MF, 1/8W, 1%, 78.7	RN55D
R26 R27 R29 R31	RES, MF, 1/4W, 1%, 196	RN60D
R3 R4 R5	RES MODULE, 10K	4310R
R6 R7	RES MODULE	4116R
R1 R2	RES MODULE, 4.7K	4116R
R8	RES MODULE	699-1
CR3	DIODE	1N746
CR4 CR5 CR6 CR7	DIODE	1N4148
CR1 CR2	DIODE	5082-
Q6	TRANS	2N2369
Q9	TRANS	2N3646
Q8	TRANS	2N3906
Q3	TRANS	2N3906
Q5	TRANS	2N4250
Q7	TRANS	2N5400

WAVETEK PARTS LIST	TITLE
	PCA, CLOCK OSC

NOTE UNLESS OTHERWISE SPECIFIED

EI SHOP GRAPHICS/ACCUPRESS
DRAWING NO. A-3886

REV	ECN	BY	DATE	APP

...GR-PART-NO	MFGR	WAVETEK NO	QTY/PT	REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	SPECT	4600-12-0300	1						
	SPECT	4600-15-0102	1	Q1	TRANS	2N5485	MOT	4901-05-4850	1
1001F	TRW	4701-03-1001	8	Q2 Q4	TRANS	J177	SILX	4902-00-1770	2
				U13B	IC	TL083CN	TI	7000-00-8300	1
1002F	TRW	4701-03-1002	1	VR1	VOLTAGE REGULATOR	LM337T	NAT	7000-03-3700	1
1210F	TRW	4701-03-1210	4	U1A U2A U3A U4A	IC	MLM339P	MOT	7000-03-3900	4
1211F	TRW	4701-03-1211	1	U11A U12B	IC, OP-AMP	LF356N	NSC	7000-03-5600	2
1240F	TRW	4701-03-1240	1	U6A	IC	AD 561 J	AD	7000-05-6100	1
1501F	TRW	4701-03-1501	3	U12C	IC	CA3140S	RCA	7000-31-4001	1
2001F	TRW	4701-03-2001	3	U1C	IC	CD4093BE	RCA	8000-40-9300	1
2490F	TRW	4701-03-2490	2	U2C	IC	F4555B	FAIR	8000-45-5500	1
2491F	TRW	4701-03-2491	1	U5B U7B	IC	74LS09	TI	8000-74-0910	2
2740F	TRW	4701-03-2740	1	U9A U9B	IC	F10010	FAIR	8001-00-1000	2
3329F	TRW	4701-03-3329	1	U7A	IC	MC10135	MOT	8001-01-3500	1
3921F	TRW	4701-03-3921	1	U8A	IC	MC10231	MOT	8001-02-3100	1
4990F	TRW	4701-03-4990	1	U1B U2B U3B	IC	74C374	NAT	8007-43-7430	3
4991F	TRW	4701-03-4991	1	U4B U6B U8B	IC	74LS490	TI	8007-44-9010	3

ASSEMBLY NO.	REV	WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
1100-00-0693			PCA, CLOCK OSC	1100-00-0693	
PAGE 3				PAGE 5	

...FGR-PART-NO	MFGR	WAVETEK NO	QTY/PT	REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
-6342F	TRW	4701-03-6342	1	U10B	IC	F100101	FAIR	8100-00-0004	1
-7BR7F	TRW	4701-03-7879	15	U10A	IC	F100107	FAIR	8100-00-0005	1
-1960F	TRW	4701-13-1960	4						
-101-103	BOURN	4770-00-0008	3						
-001-102	BOURN	4770-00-0019	2						
-001-472	BOURN	4770-00-0020	2						
R2K(B)	BECK	4770-00-0021	1						
A	FAIR	4801-01-0746	1						
8	FAIR	4807-02-6666	4						
-2811	MP	4809-02-2811	2						
9A	MOT	4901-02-3691	1						
6	NSC	4901-03-6460	1						
3	NSC	4901-03-9030	1						
5	ITT	4901-03-9050	1						
8	NSC	4901-04-2580	1						
4	MOT	4901-05-4840	1						

ASSEMBLY NO.	REV	WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
1100-00-0693			PCA, CLOCK OSC	1100-00-0693	
PAGE 4				PAGE 6	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, CLOCK OSC.
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 1100-00-0693 REV H
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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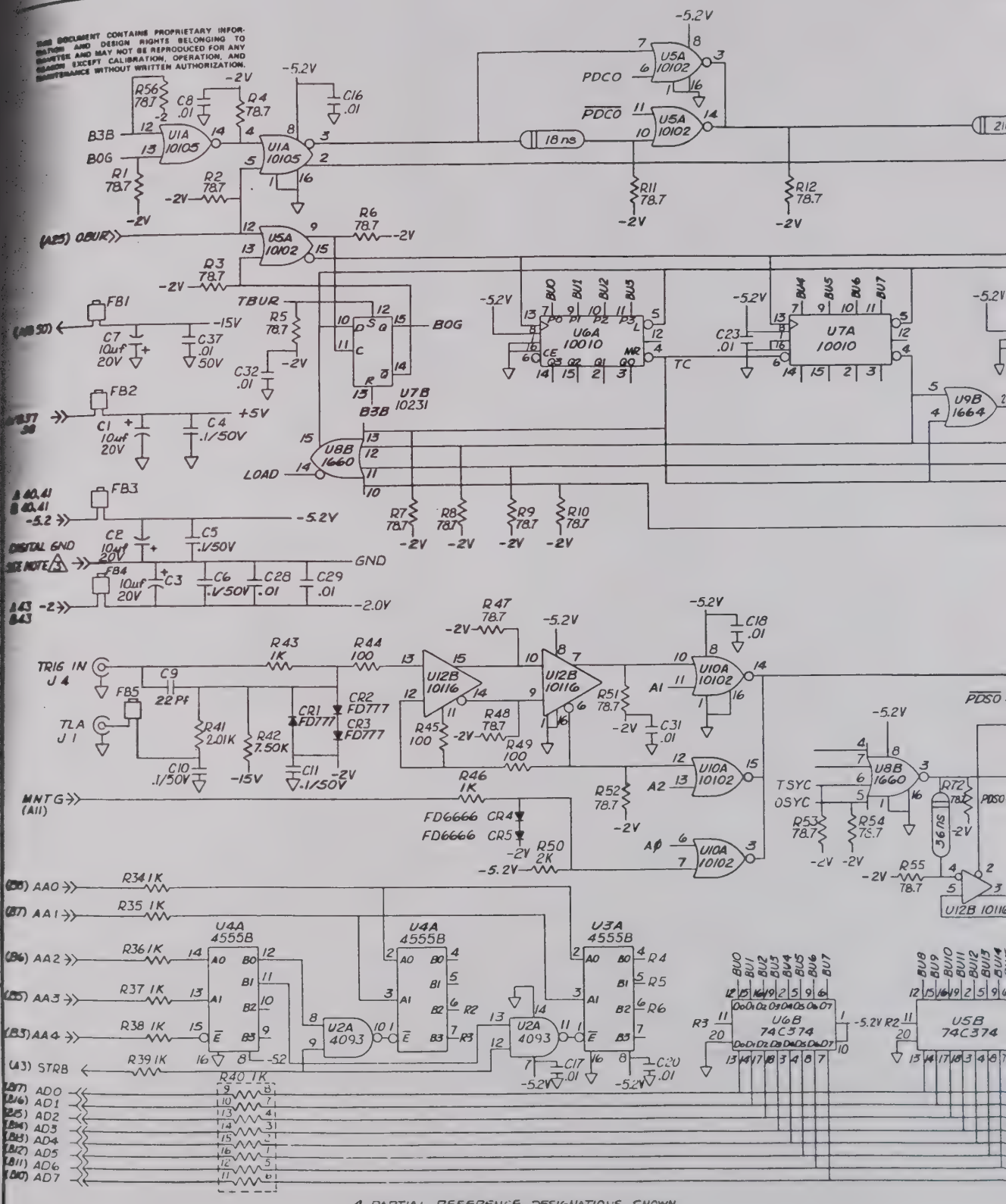


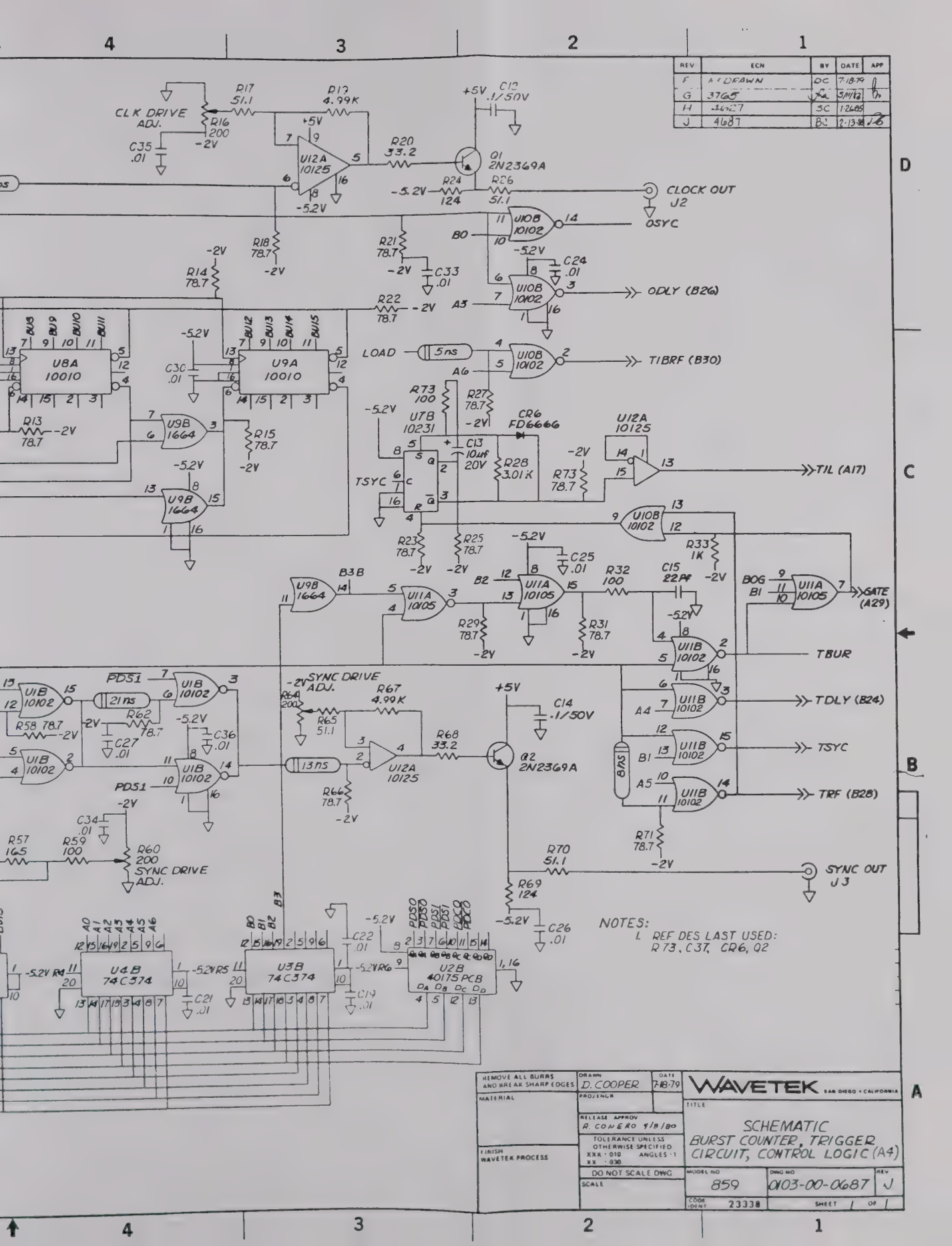
4. PARTIAL REFERENCE DESIGNATIONS SHOWN, PREFIX WITH ASSEMBLY REF DES A4.

B 25,27,29,31
AB 19,21,23,32,33,34,35
A 24,26,28,30

2. ALL RESISTORS IN OHMS; 1/8 W, 1%

1. ALL CAPACITORS IN MICROFARADS

NOTE UNLESS OTHERWISE SPECIFIED



REV | ECN | BY | DATE | APP
F | RE DRAWN | DC | 7-18-79
G | 3765 | | 5/11/82
H | 4627 | SC | 1-26-85
J | 4687 | BC | 2-13-86
CLK DRIVE ADJ.
R16 200
C35 .01
R17 51.1
R19 4.99K
U12A 10125
R20 33.2
Q1 2N2369A
C12 .1/50V
R24 124
R26 51.1
CLOCK OUT J2
OSYC
U10B 10102
R18 78.7
R21 78.7
C33 .01
C24 .01
ODLY (B26)
R14 78.7
R22 78.7
U8A 10010
U9A 10010
C30 .01
LOAD
5ns
TIBRF (B30)
R73 100
R27 78.7
U7B 10231
CR6 FD6666
C13 10uf 20V
R28 3.01K
U12A 10125
TIL (A17)
R13 78.7
U9B 1664
R15 78.7
TSYC
R23 78.7
R25 78.7
R33 1K
C25 .01
R32 100
C15 22PF
U11A 10105
GATE (A29)
R29 78.7
R31 78.7
U11B 10102
TBUR
PDS1
21ns
R58 78.7
R62 78.7
C27 .01
C36 .01
SYNC DRIVE ADJ.
R64 200
R65 51.1
R67 4.99K
R68 33.2
Q2 2N2369A
C14 .1/50V
TDLY (B24)
TSYC
TRF (B28)
8ns
13ns
R66 78.7
C34 .01
R57 165
R59 100
R60 200 SYNC DRIVE ADJ.
R71 78.7
R70 51.1
SYNC OUT J3
R69 124
C26 .01
U4B 74C374
U3B 74C374
U2B 40175 PCB
C21 .01
C22 .01
C19 .01
NOTES:
1. REF DES LAST USED: R73, C37, CR6, Q2
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER
DATE 7-18-79
PROJENGR
RELEASE APPROV R. CONERO 9/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC BURST COUNTER, TRIGGER CIRCUIT, CONTROL LOGIC (A4)
MODEL NO 859
DWG NO 0103-00-0687
REV J
CODE IDENT 23338
SHEET 1 OF 1

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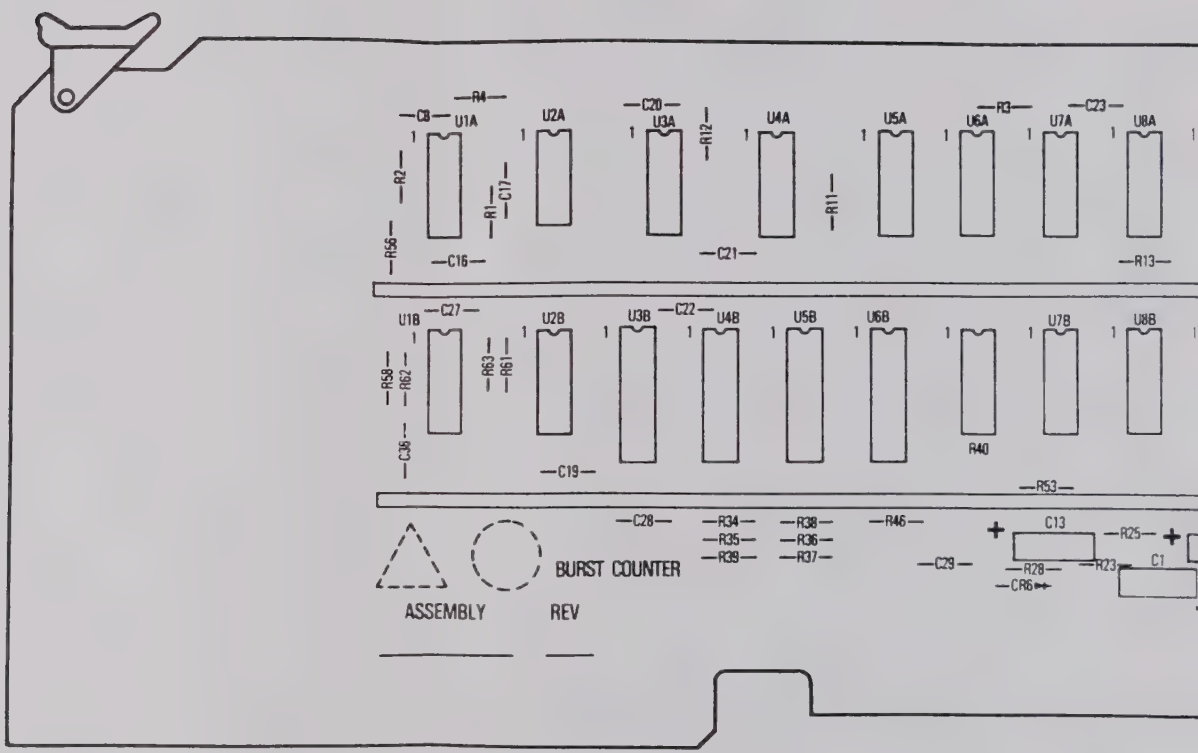
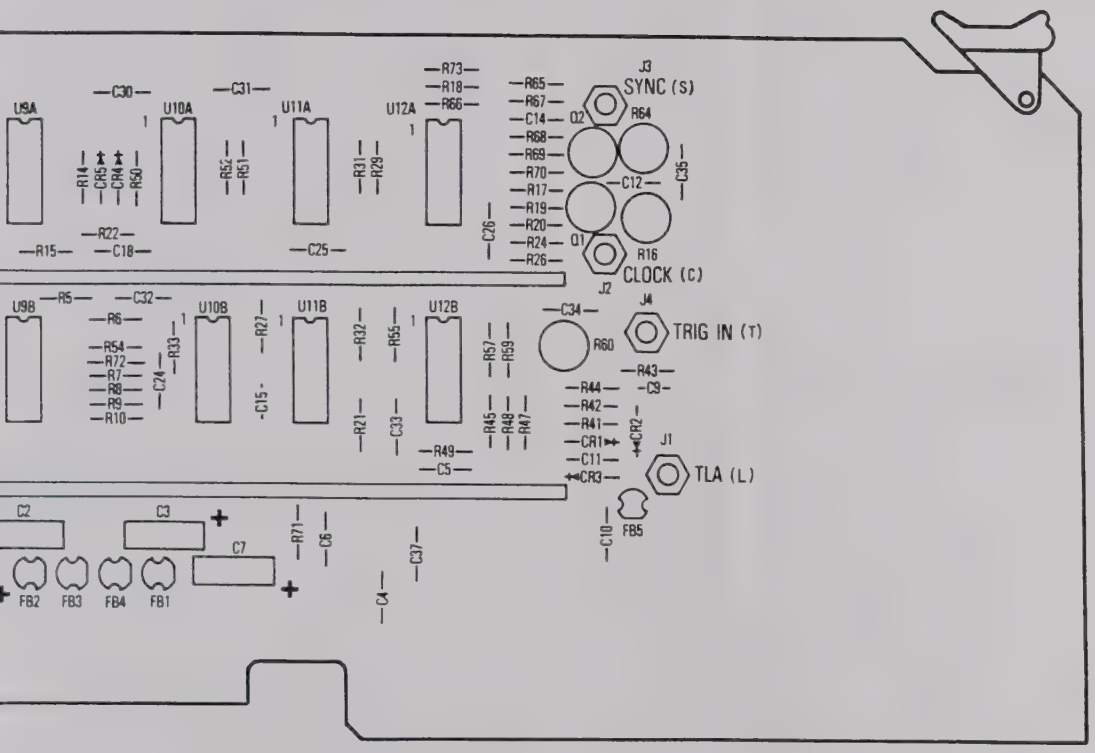
WAVETEK AND MAY NOT BE REPRODUCED FOR ANY
REASON EXCEPT CALIBRATION OPERATION AND
MAINTENANCE WITHOUT WRITTEN AUTHORIZATION





MADE FROM 0100-00-0687-5F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: TRIGER & BURST COUNTER
FINISH: WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ± .XX ±.030		
	DO NOT SCALE DWG		
	SCALE	MODEL NO. 859	DRAWING NO. 1100-00-0687 REV. F

CONTAINS PROPRIETARY INFOR-
DESIGN RIGHTS BELONGING TO
MAY NOT BE REPRODUCED FOR ANY
CALIBRATION, OPERATION, AND
WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG, BURST BD
NONE	SCHEMATIC, BURST BD
C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C8	CAP, CER, MN, .01MF, 50V
C10 C11 C12 C14 C4 C5 C6	CAP, CER, MON, 1MF, 50V
C15 C9	CAP, CER, 22PF, 1KV
C1 C13 C2 C3 C7	CAP, TANT, 10MF, 20V
NONE	BURST BOARD
J1 J2 J3 J4	CONN
NONE	PC BD EJECTOR
NONE	WASHER, FLAT FIBRE #1
FB1 FB2 FB3 FB4 FB5	BALUN CORE
R16 R60 R64	POT, TRIM, 200
R32 R44 R45 R49 R59 R74	RES, MF, 1/8W, 1%, 100
R33 R34 R35 R36 R37 R38 R39 R43 R46	RES, MF, 1/8W, 1%, 1K
R69 R24	RES, MF, 1/8W, 1%, 124

WAVETEK PARTS LIST	TITLE
	PCA, BURST BOARD

REFERENCE DESIGNATORS	PART DESCRIPTION
R57	RES, MF, 1/8W, 1%, 165
R41 R50	RES, MF, 1/8W, 1%, 2K
R28	RES, MF, 1/8W, 1%, 3.01K
R20 R68	RES, MF, 1/8W, 1%, 33.2
R19 R67	RES, MF, 1/8W, 1%, 4.99K
R17 R26 R65 R70	RES, MF, 1/8W, 1%, 51.1
[illegible]	RES, MF, 1/8W, 1%, 7.5K
R1 R10 R11 R12 R13 R14 R15 R18 R2 R21 R22 R23 R25 R27 R29 R3 R31 R4 R47 R48 R5 R51 R52 R53 R54 R55 R56 R58 R6 R62 R66 R7 R71 R72 R73 R8 R9	RES, MF, 1/8W, 1%, 78.7
R40	RES MODULE
CR1 CR2 CR3	DIODE
CR4 CR5 CR6	DIODE
Q1 Q2	TRANS
NONE	BUSS BAR
U8B	IC

WAVETEK PARTS LIST	TITLE
	PCA, BURST BOARD

UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
0101-00-0687	WVTK	0101-00-0687	1
0103-00-0687	WVTK	0103-00-0687	1
GE50-103ZA	MURAT	1500-01-0310	23
CAC03Z5U104Z050A	CORNG	1500-01-0405	7
DD-220	CRL	1500-02-2011	2
150D106X9020B2	SPRAG	1500-71-0601	5
859-0687	WVTK	1700-00-0687	1
27-848	AMPH	2100-07-0011	4
103 GREEN	CALMK	2800-07-0013	2
5602-4-32	SESTM	2800-28-0006	4
2873000902	FARIT	3100-00-0002	5
91AR200	BECK	4600-02-0101	3
RN55D-1000F	TRW	4701-03-1000	6
RN55D-1001F	TRW	4701-03-1001	9
55D-1240F	TRW	4701-03-1240	2

ASSEMBLY NO.	REV
1100-00-0687	

PAGE 1

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
RN55D-1650F	TRW	4701-03-1650	1
RN55D-2001F	TRW	4701-03-2001	2
RN55D-3011F	TRW	4701-03-3011	1
RN55D-33R2F	TRW	4701-03-3329	2
RN55D-4991F	TRW	4701-03-4991	2
RN55D-51R1F	TRW	4701-03-5119	4
RN55D-7501F	TRW	4701-03-7501	1
RN55D-78R7F	TRW	4701-03-7879	37
4116R-001-102	BOURN	4770-00-0019	1
FD777	FAIR	4807-02-0777	3
1N4148	FAIR	4807-02-6666	3
2N2369A	MOT	4901-02-3691	2
6009-90-0009	WVTK	6009-90-0009	2
MC1660	MOT	8000-16-6000	1

ASSEMBLY NO	REV
1100-00-0687	

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U9B	IC	MC1664	MOT	8000-16-6400	1
U2A	IC	CD4093BE	RCA	8000-40-9300	1
U3A U4A	IC	F4555B	FAIR	8000-45-5500	2
U6A U7A U8A U9A	IC	F10010	FAIR	8001-00-1000	4
U10A U10B U11B U1B U5A	IC	MC10102	MOT	8001-01-0200	5
U11A U1A	IC	MC10105	MOT	8001-01-0500	2
U12B	IC	MC10116P	MOT	8001-01-1600	1
U12A	IC	MC10125P	MOT	8001-01-2500	1
U7B	IC	MC10231	MOT	8001-02-3100	1
U2B	IC	40175	NAT	8004-01-7500	1
U3B U4B U5B U6B	IC	74C374	NAT	8007-43-7430	4

ASSEMBLY NO	REV
1100-00-0687	

PAGE 3

WAVETEK PARTS LIST

TITLE: PCA, BURST BOARD

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, BURST BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG		MODEL NO: 859 — DWG NO: 1100-00-0687 — REV: F
	SCALE		CODE IDENT: 23338 — SHEET 1 OF 1

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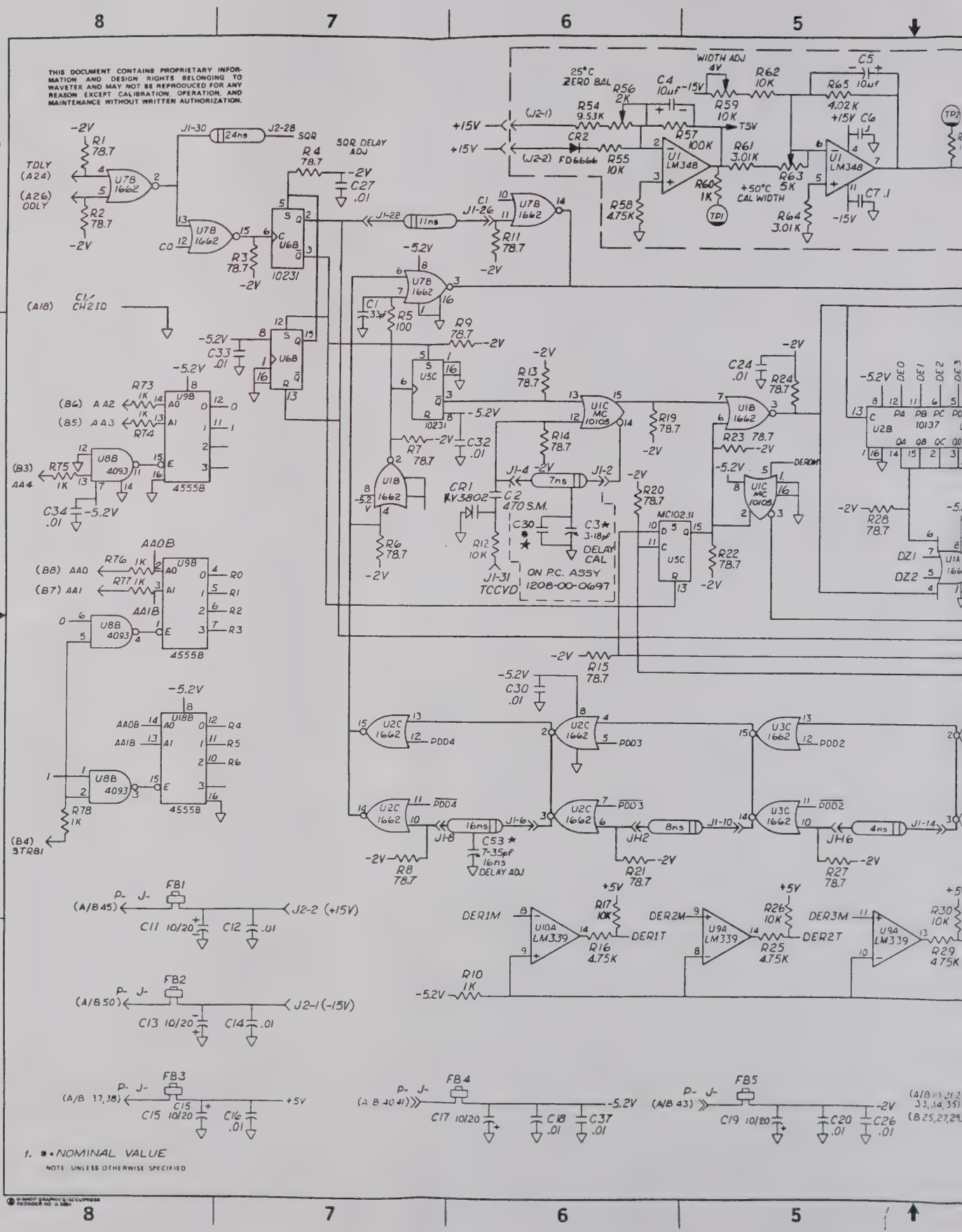

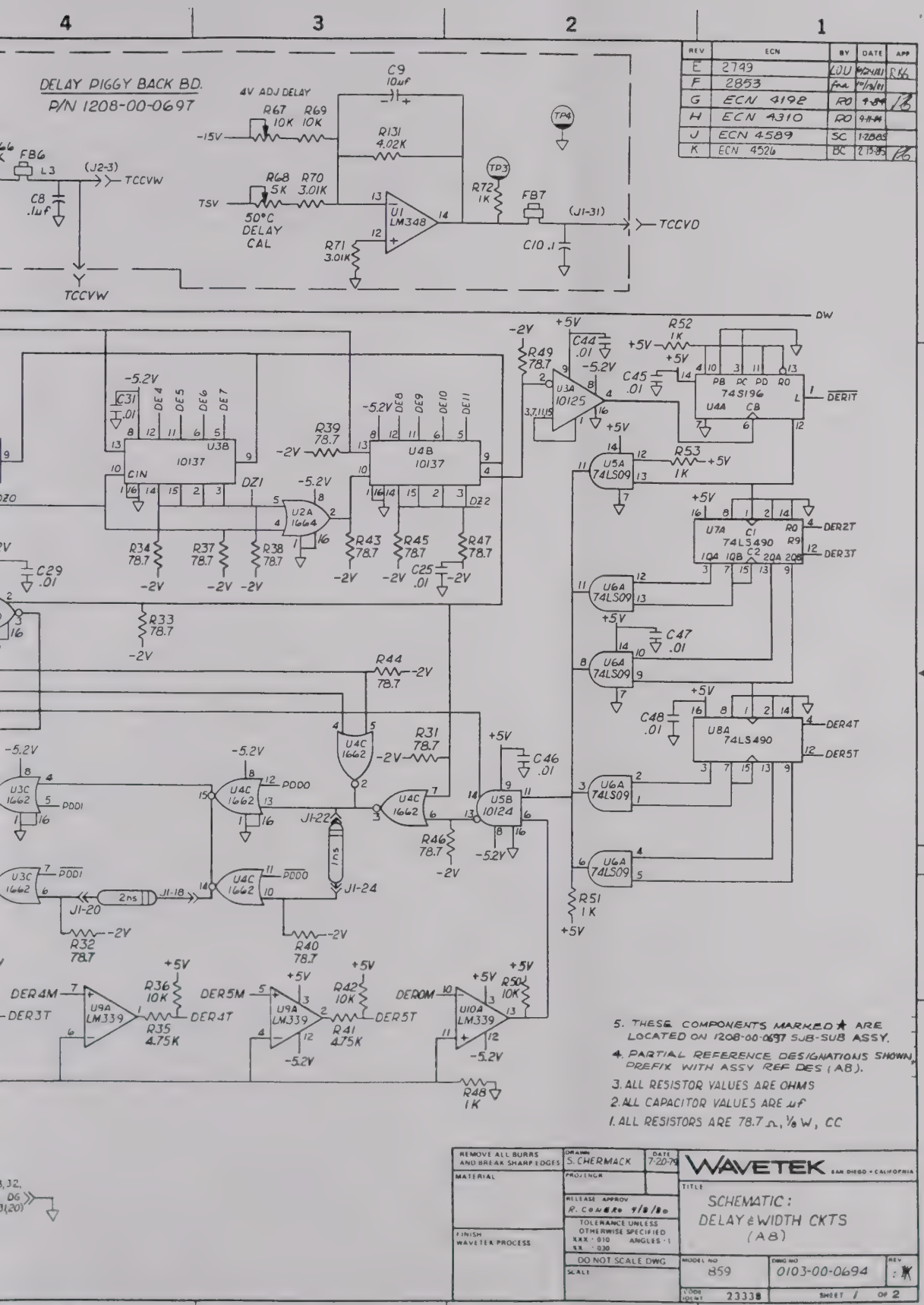

REV	ECN	BY	DATE	APP
E	2749	LOU	9/24/81	RBG
F	2853	fra	10/13/81	
G	ECN 4192	RO	4-8-84	
H	ECN 4310	RO	9-11-84	
J	ECN 4589	SC	1-28-85	
K	ECN 4526	BC	2-15-85	

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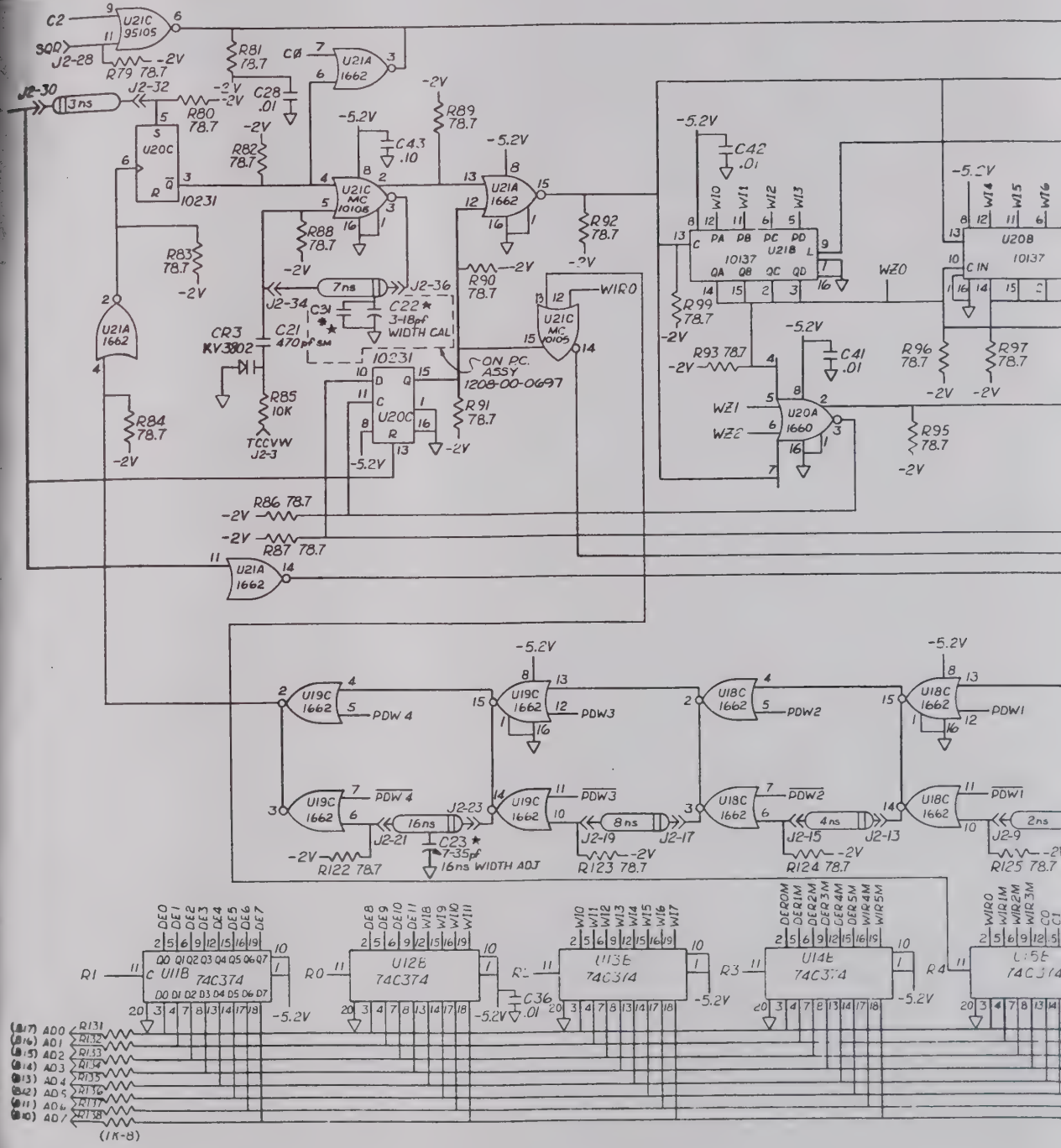

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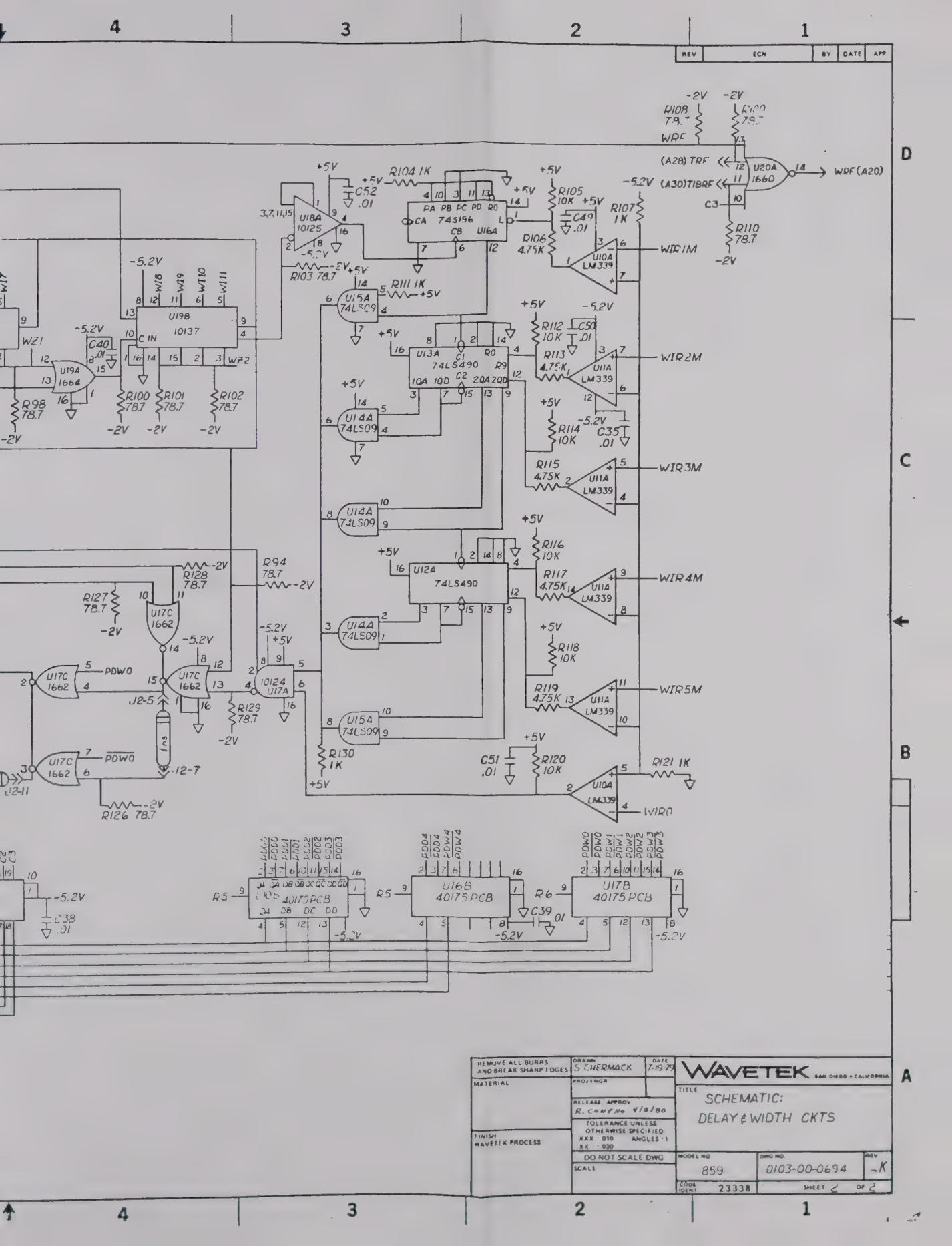

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 7-19-79	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC: DELAY & WIDTH CKTS
	RELEASE APPROV R. CONFRO 4/8/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 XX ± .030 ANGLES ± 1		
	DO NOT SCALE DWG		MODEL NO 859 / DWG NO. 0103-00-0694 / REV -K
	SCALE		CODE IDENT 23338 / SHEET 2 OF 2

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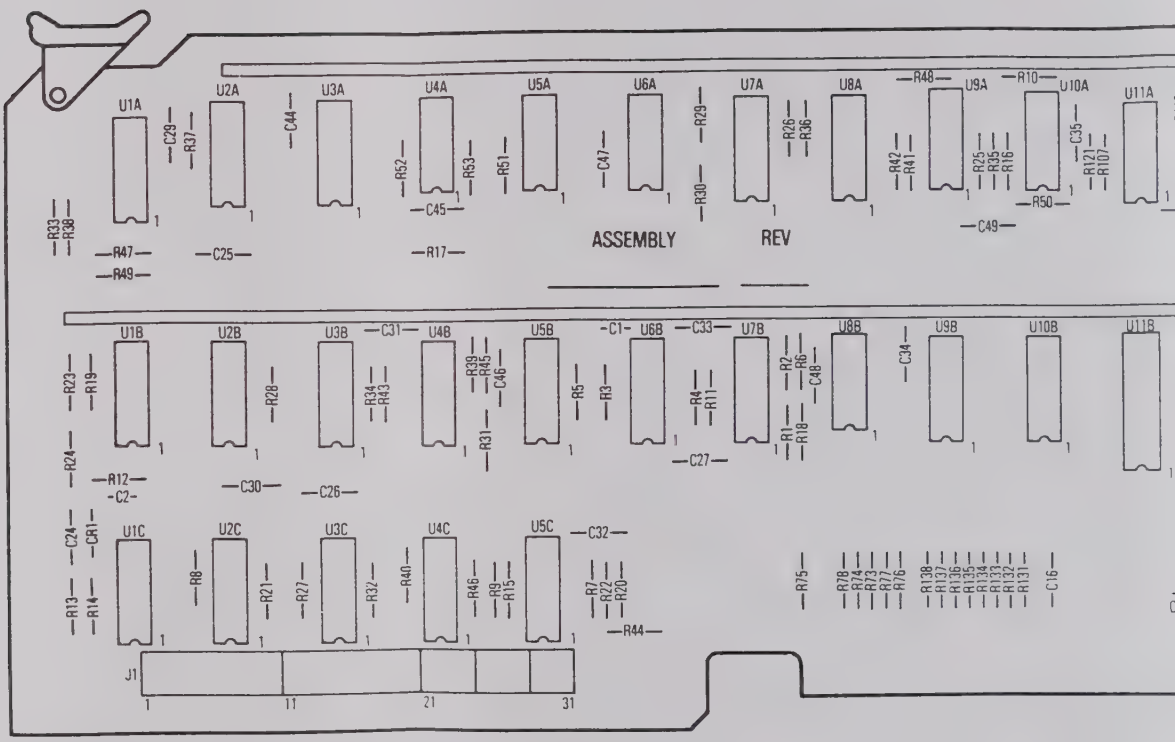
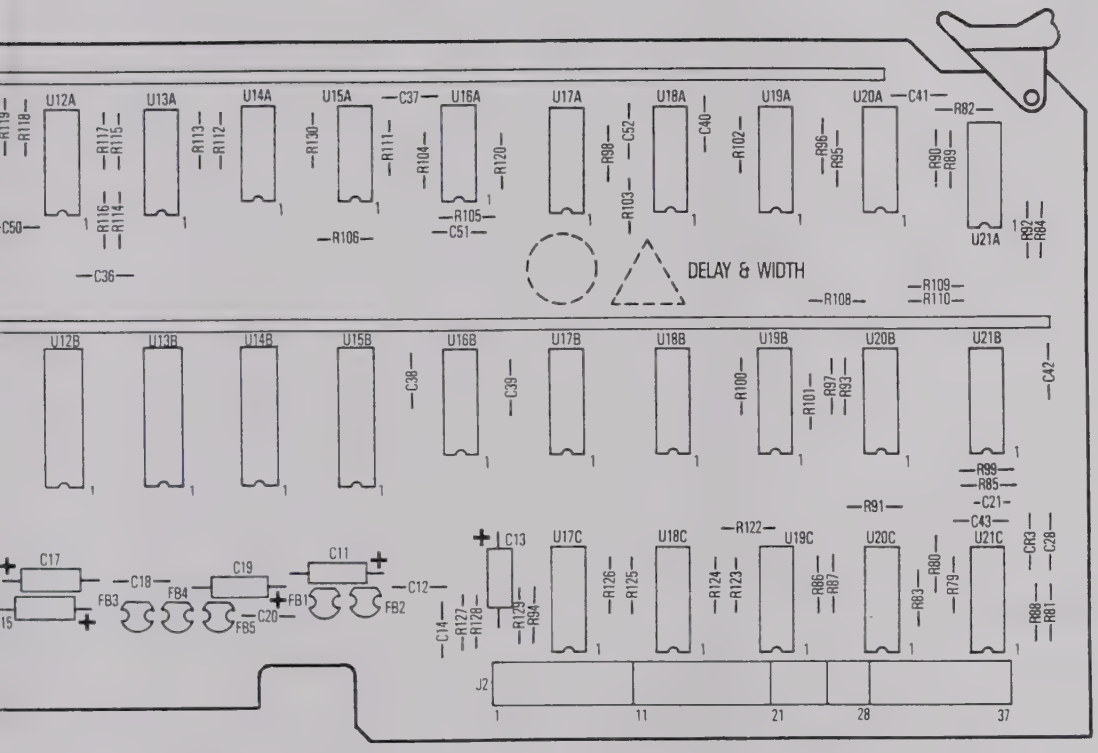
MAINTENANCE WITHOUT WRITTEN AUTHORIZATION





MADE FROM 0100-00-0694-5D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK
MATERIAL	PROJ ENGR		TITLE: DELAY & WIDTH
FINISH: WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED		
	DO NOT SCALE DWG		
			859 / 1100-00-0694 / D
			23338 / SHEET 1 OF 1

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REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG, DELAY/WI
NONE	SCHEMATIC, DELAY/WI
NONE	PCA, DELAY PIGGY'BK
C12 C14 C16 C18 C20 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C34 C35 C36 C37 C38 C39 C40 C41 C42 C43 C44 C45 C46 C47 C48 C49 C50 C51 C52	CAP, CER, MN, .01MF, 3
C1	CAP, CER, 33PF, 1KV
C2 C21	CAP, MICA, 470PF, 500
C11 C13 C15 C17 C19	CAP, TANT, 10MF, 20V
NONE	DELAY/WIDTH
NONE	CONN
NONE	CONN
NONE	CONN PC.
NONE	PC BD EJECTOR
FB1 FB2 FB3 FB4 FB5	BALUN CORE
R5	RES, MF, 1/8W, 1%, 100
R10 R104 R107 R111 R121	RES, MF, 1/8W, 1%, 1K

WAVETEK PARTS LIST	TITLE: PCA, DELAY/WIDTH BD

REFERENCE DESIGNATORS	PART DESCRIPTION
R130 R131 R132 R133 R134 R135 R136 R137 R138 R48 R51 R52 R53 R73 R74 R75 R76 R77 R78	
R105 R112 R114 R116 R118 R12 R120 R17 R26 R30 R36 R42 R50 R85	RES, MF, 1/8W, 1%, 10K
R106 R113 R115 R117 R119 R16 R25 R29 R35 R41	RES, MF, 1/8W, 1%, 4.7
R1 R100 R101 R102 R103 R108 R109 R11 R110 R122 R123 R124 R125 R126 R127 R128 R129 R13 R14 R15 R19 R2 R20 R21 R22 R23 R24 R27 R28 R3 R31 R32 R33 R34 R37 R38 R39 R4 R40 R43 R44 R45 R46 R47 R49 R6 R7 R79 R8 R80 R81 R82 R83 R84 R86 R87 R88 R89 R9 R90 R91 R92 R93 R94 R95 R96 R97 R98 R99	RES, MF, 1/8W, 1%, 78
CR1 CR3	DIODE
NONE	POWER BUSS BAR (LO
NONE	POWER BUS BAR
U10A U11A U9A	IC
U1A U20A	IC

WAVETEK PARTS LIST	TITLE: PCA, DELAY/WIDTH BD

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	0101-00-0694	WVTK	0101-00-0694	1
	0103-00-0694	WVTK	0103-00-0694	1
	859-0697	WVTK	1208-00-0697	1
V	GE50-103ZA	MURAT	1300-01-0310	34
	DD-330	CRL	1300-03-3011	1
	DM15-471J	ARCO	1300-14-7100	2
	150D106X9020B2	SPRAG	1300-71-0601	5
	859-0694	WVTK	1700-00-0694	1
	22-17-2042	MOLEX	2100-02-0065	3
	22-17-2032	MOLEX	2100-02-0066	2
	22-17-2102	MOLEX	2100-02-0089	5
	103 BLUE	CALMK	2800-07-0014	2
	2873000902	FARIT	3100-00-0002	5
	RN55D-1000F	TRW	4701-03-1000	1
	RN55D-1001F	TRW	4701-03-1001	24

	ASSEMBLY NO.	REV
	1100-00-0694	

PAGE 1

	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	RN55D-1002F	TRW	4701-03-1002	14
K	RN55D-4751F	TRW	4701-03-4751	10
	RN55D-78R7F	TRW	4701-03-7879	69
	KV3902	KSW	4803-02-3802	2
	6009-90-0004	WVTK	6009-90-0004	1
	6009-90-0007	WVTK	6009-90-0007	1
	MLM339P	MOT	7000-03-3900	3
	MC1660	MOT	8000-16-6000	2

	ASSEMBLY NO	REV
	1100-00-0694	

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U17C U18C U19C U1B U21A U2C U3C U4C U7B	IC	MC1662	MOT	8000-16-6200	9
U19A U2A	IC	MC1664	MOT	8000-16-6400	2
[illegible]	IC	CD4093BE	RCA	8000-40-9300	1
U18B U9B	IC	F4555B	FAIR	8000-45-5500	2
U14A U15A U5A U6A	IC	74LS09	TI	8000-74-0910	4
U1C U21C	IC	MC10105	MOT	8001-01-0500	2
U17A U5B	IC	MC10124P	MOT	8001-01-2400	2
U18A U3A	IC	MC10125P	MOT	8001-01-2500	2
U19B U20B U21B U2B U3B U4B	IC	MC10137	MOT	8001-01-3700	6
U20C U5C U6B	IC	MC10231	MOT	8001-02-3100	3
U10B U16B U17B	IC	40175	NAT	8004-01-7500	3
U16A U4A	IC	SN74S196J	TI	8007-41-9601	2
U11B U12B U13B U14B U15B	IC	74C374	NAT	8007-43-7430	5
U12A U13A U7A U8A	IC	74LS490	TI	8007-44-9010	4

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA. DELAY/WIDTH BD	1100-00-0694	

PAGE 3

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
	RELEASE APPROV		PARTS LIST PCA, DELAY/WIDTH BC.
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 1100-00-0694 REV D
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

4 3 2 1

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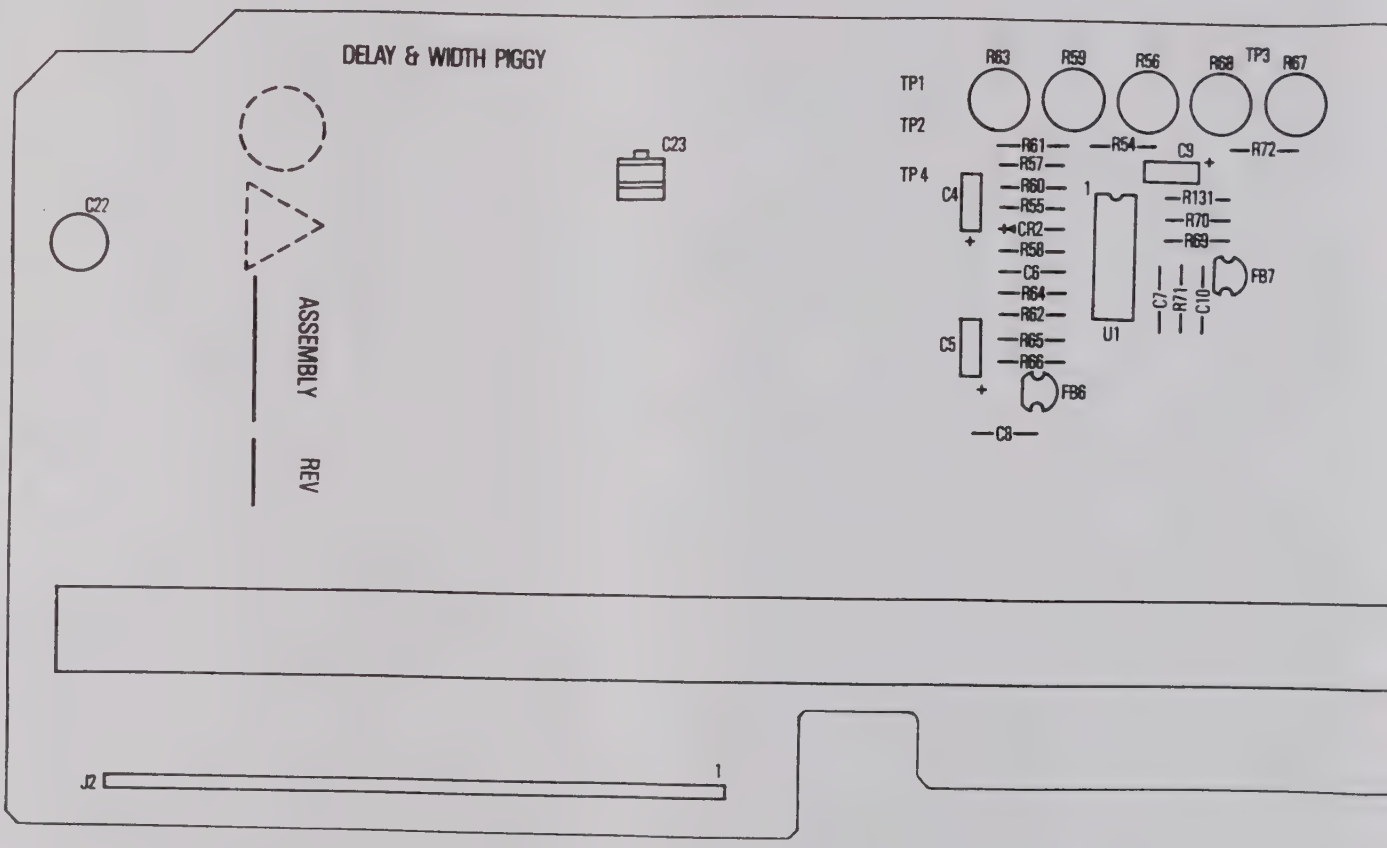

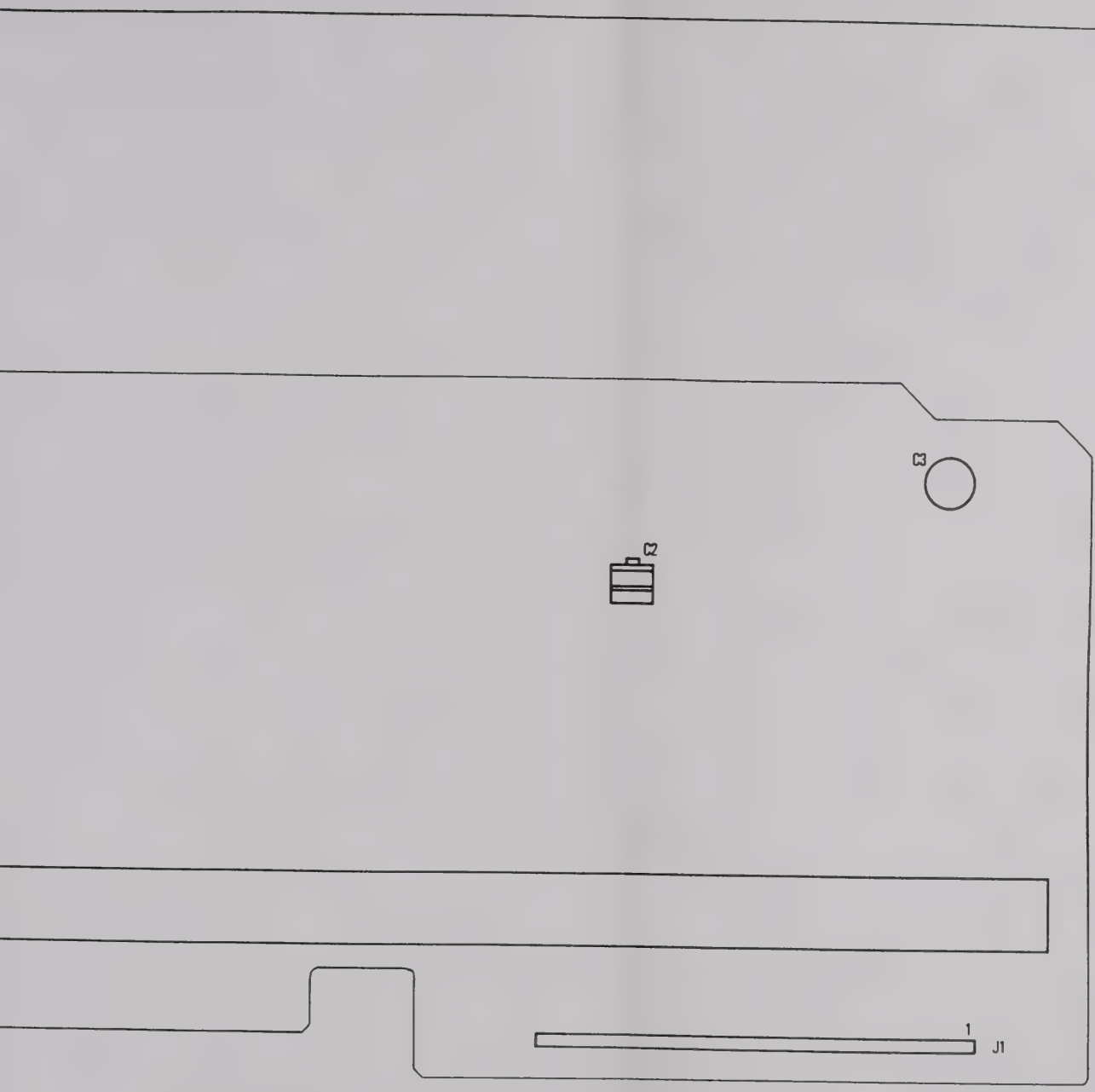

MADE FROM 0100-00-0697-3E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE
	RELEASE APPROV		DELAY & WIDTH PIGGYBACK
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± XX ± .030		
	DO NOT SCALE DWG	MODEL NO. 859	DWG NO. 1208-00-0697 REV E
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DELAY	0101-00-0697	WVTK	0101-00-0697	1
NONE	SCHEMATIC, DELAY/MID	0103-00-1260	WVTK	0103-00-1260	1
NONE	STIFFENER, PC	859-9030	WVTK	1400-00-9030	1
C30T	CAP, CER, 10PF, 1KV	DD-100LL	CRL	1500-01-0001	1
C10 C6 C7 C8	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	4
C31T	CAP, CER, 33PF, 1KV	DD-330 LONG LEAD	CRL	1500-03-3001	1
C22 C3	CAP, VAR, 3-18PF	GKU18000	SPRAG	1500-51-8010	2
C2 C23	CAP, VARI, 7-35PF, 250V	7S TRIKO-22, 7/35PF	TRIKO	1500-53-5010	2
C4 C5 C9	CAP, TANT, 10MF, 20V	150D106X9020B2	SPRAG	1500-71-0601	3
NONE	DELAY/WIDTH PIGGYB'K	859-0697	WVTK	1700-00-0697	1
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
NONE	CONN PIN, MALE (UOM-EA PIN)	CA-S365P-100-230-830	CA	2100-05-0034	68
NONE	STANDOFF, SWAGE 312 H, 187 HEX2-56, 062 MAT'L	SS158-3B-5	UNICP	2800-02-0028	9
FB6 FB7	BALUN CORE	2873000902	FARIT	3100-00-0002	2
R59 R67	POT, TRIM, 10K	91AR10K	BECK	4600-01-0315	2

WAVETEK PARTS LIST	TITLE: PCA, DELAY PIGGY'BK	ASSEMBLY NO.: 1208-00-0697	REV
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R56	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	1
R63 R68	POT, TRIM, 5K	91AR5K	BECK	4600-05-0205	2
R60 R66 R72	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	3
R55 R62 R69	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	3
R57	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	1
R61 R64 R70 R71	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	4
R101 R65	RES, MF, 1/8W, 1%, 4.02K	RN55D-4021F	TRW	4701-03-4021	2
R58	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	1
R54	RES, MF, 1/8W, 1%, 9.53K	RN55D-9531F	TRW	4701-03-9531	1
CR2	DIODE	1N4148	FAIR	4807-02-6666	1
U1	IC	LM348N	NSC	7000-03-4800	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.: 1208-00-0697	REV
	PCA, DELAY PIGGY'BK	PAGE 2	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, DELAY PIGGYBACK
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO: 859	DWG NO: 1208-00-0697 REV: G
	SCALE	CODE IDENT: 23338	SHEET 1 OF 1

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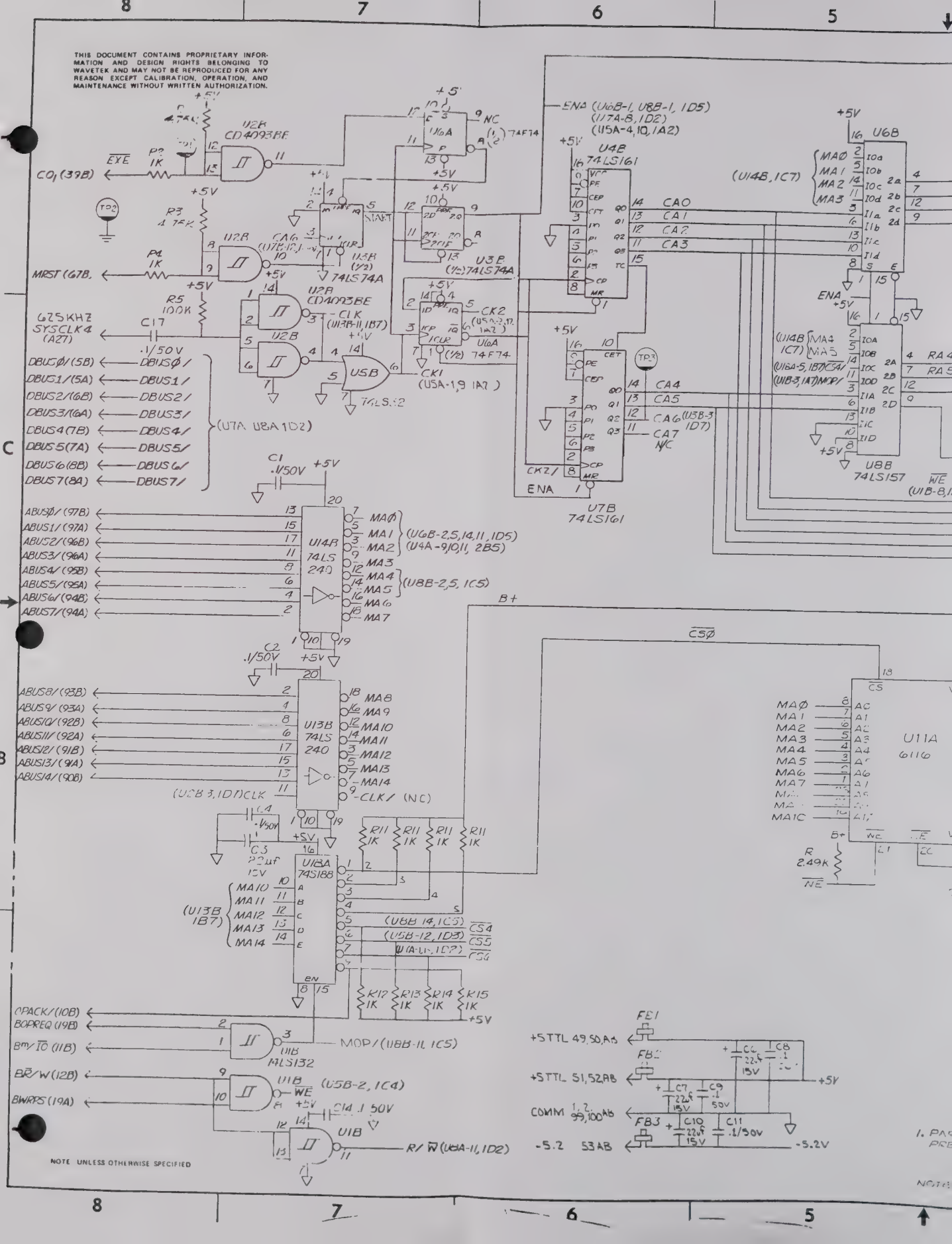

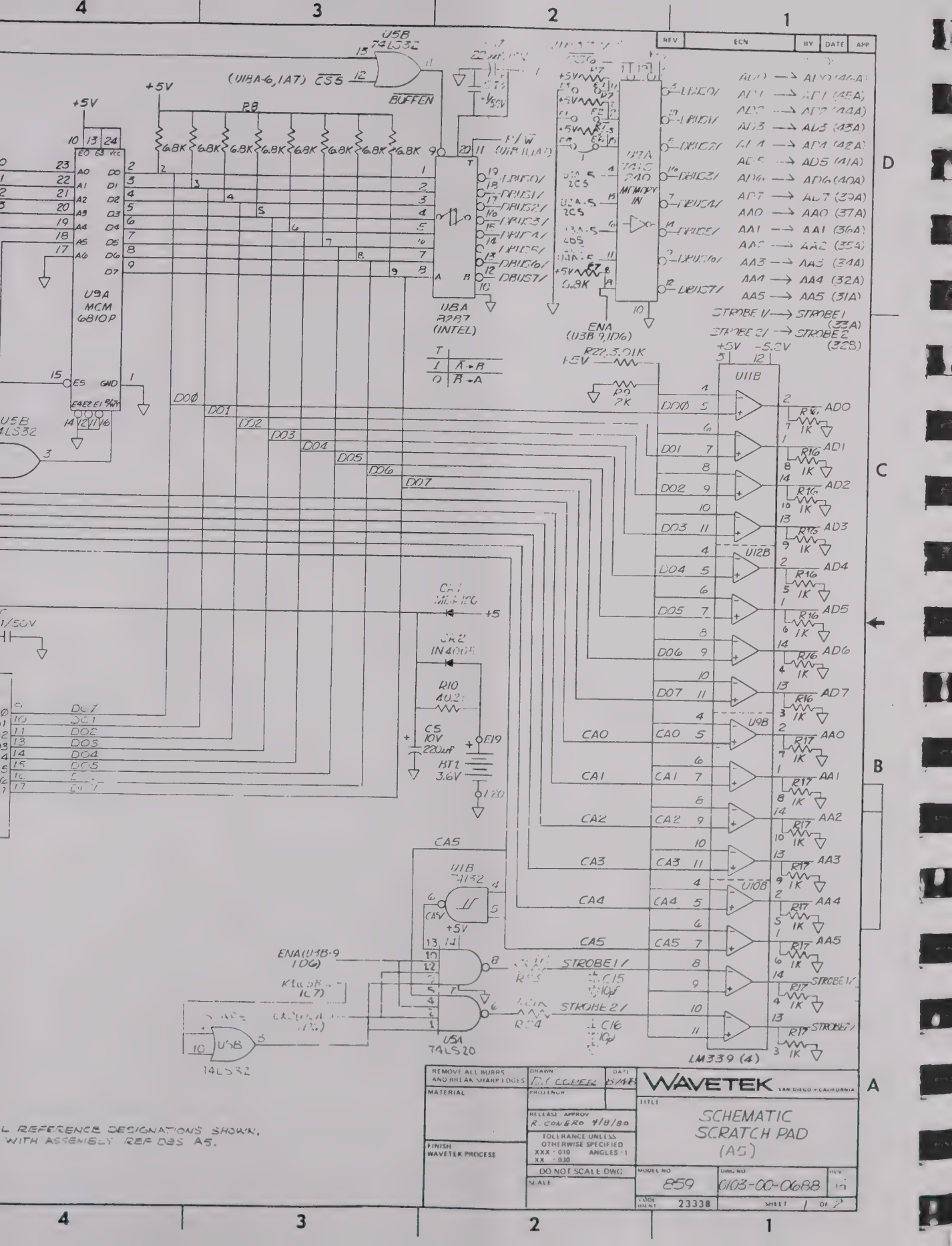

U5B 74LS32
(U1BA-6,1A7) CS5
BUFFEN
+5V
R8
6.8K
U9A MCM 6810P
U8A 8287 (INTEL)
U7A 74LS 240 MEMORY IN
ENA (U3B 9,1D6)
AD0 → AD0 (46A)
AD1 → AD1 (45A)
AD2 → AD2 (44A)
AD3 → AD3 (43A)
AD4 → AD4 (42A)
AD5 → AD5 (41A)
AD6 → AD6 (40A)
AD7 → AD7 (39A)
AA0 → AA0 (37A)
AA1 → AA1 (36A)
AA2 → AA2 (35A)
AA3 → AA3 (34A)
AA4 → AA4 (32A)
AA5 → AA5 (31A)
STROBE 1/ → STROBE 1 (33A)
STROBE 2/ → STROBE 2 (32B)
R22 3.01K
R9 2K
U11B
U12B
U9B
U10B
R16 1K
R17 1K
CR1 MER 120
CR2 1N4005
R10 40.2
C5 10V 220uf
BT1 3.6V
E19
E20
CA5
U1B 74132
ENA (U3B-9 1D6)
STROBE 1/
STROBE 2/
C15 10pf
C16 10pf
U5A 74LS20
U5B 74LS32
LM339 (4)
L REFERENCE DESIGNATIONS SHOWN.
WITH ASSEMBLY REF DES A5.
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D.C. COPER
DATE 8/4/78
PROJ ENGR
RELEASE APPROV R. CONGRO 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE SCHEMATIC SCRATCH PAD (A5)
MODEL NO 859
DWG NO 0103-00-0688
REV G
CODE IDENT 23338
SHEET 1 OF 2

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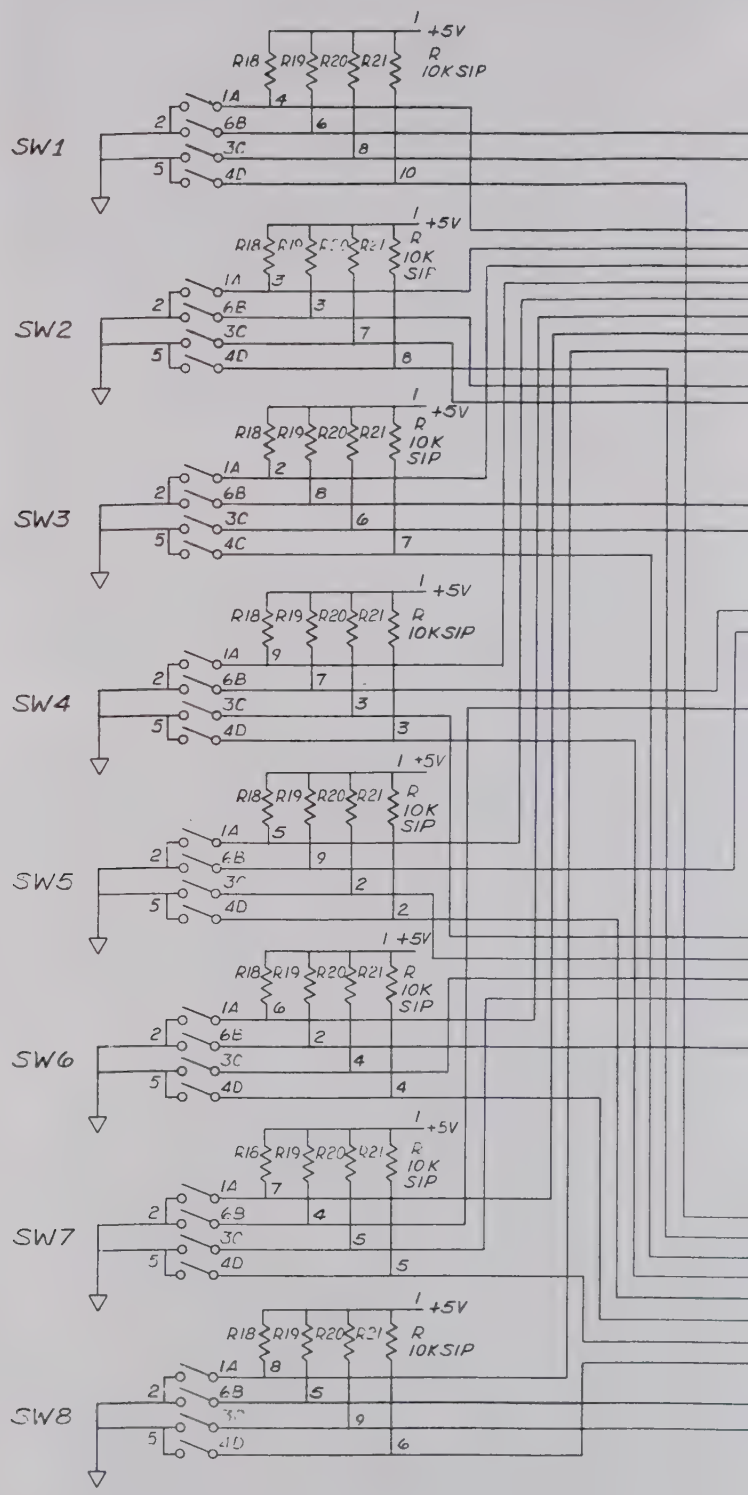

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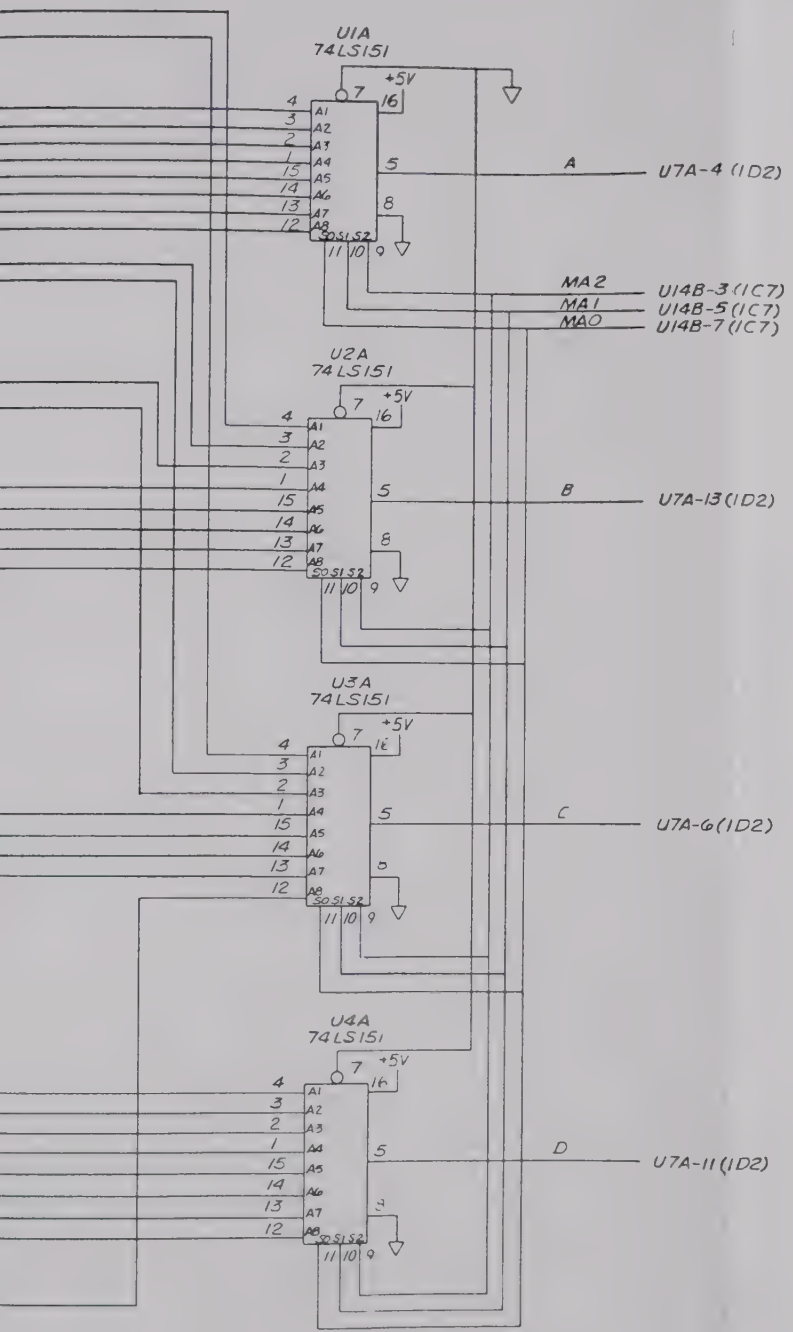


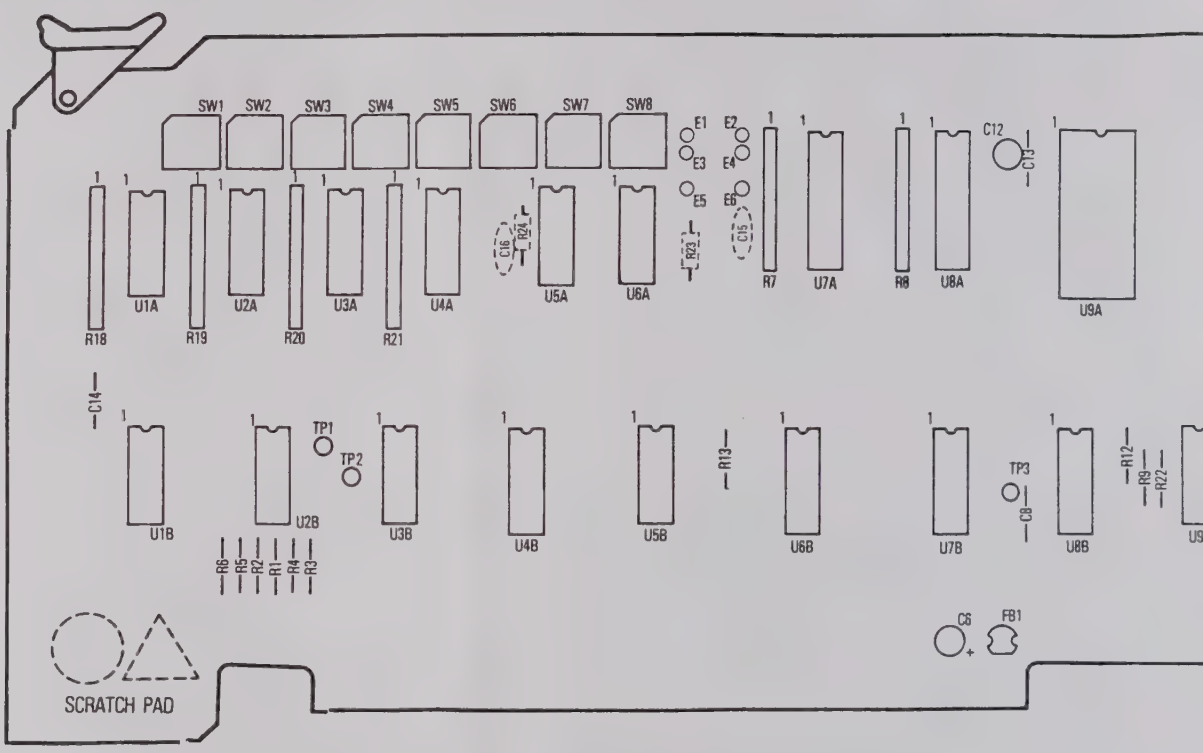
REV	ECN	BY	DATE	APP
B	2314	[illegible]	9-1-81	
C	3240	fra	7/9/82	
D	4460	SGC	8-17-83	
E	7135	[illegible]	4/1/86	
F	7549	[illegible]	7/20/86	
G	7526	BR	11/6/86	SS

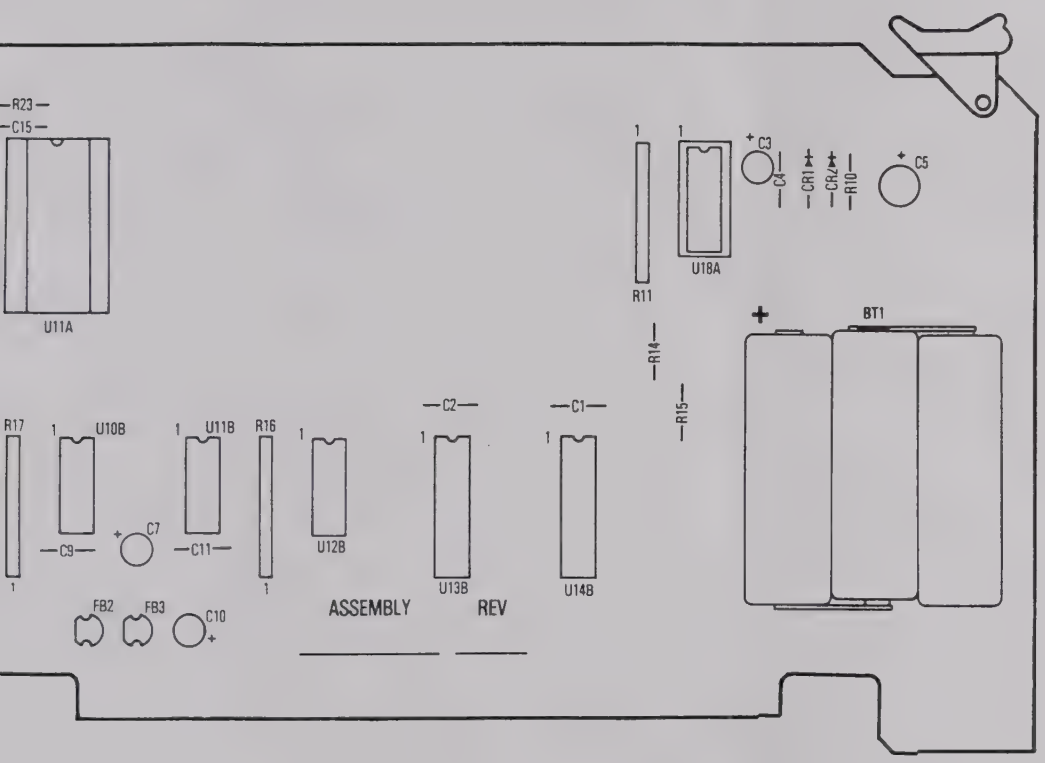
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER DATE 7-20-79
PROJENGR
RELEASE APPROV R. CONGER 4/8/80
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
SCHEMATIC SCRATCH PAD

MODEL NO 1154
DWG NO 0103-00-0155
REV G
CODE IDENT 23338
SHEET 2 OF 2


SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
E1
E2
E3
E4
E5
E6
C12
C13
C14
C15
C16
R7
R8
R18
R19
R20
R21
R23
U1A
U2A
U3A
U4A
U5A
U6A
U7A
U8A
U9A
U1B
U2B
U3B
U4B
U5B
U6B
U7B
U8B
TP1
TP2
TP3
R1
R2
R3
R4
R5
R6
R9
R12
R13
R22
C8
C6
FB1
SCRATCH PAD



MADE FROM 0100-00-0688-3E

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: SCRATCH PAD RAM
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX .010 ANGLES 1 XX .030		
	DO NOT SCALE DWG	MODEL NO: 859	DWG NO: 1100-00-0688 REV
	SCALE	JOB NO: 23338	SHEET 1 OF 1

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REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG, SCRATCH
NONE	SCHEMATIC, SCRATCH
C1 C11 C13 C14 C17 C2 C4 C8 C9	CAP, CER, MON, . 1MF,
C10 C12 C3 C6 C7	CAP, TANT, 22MF, 15V
C5	CAP, TANT, 220MF, 10
NONE	SCRATCH PAD
NONE	SKT, IC, 16PIN
NONE	SKT, IC, 24PIN
TP1 TP2 TP3	BUSS BAR STANDOFF
NONE	TIE STRAP
4	PC BD EJECTOR
FB1 FB2 FB3	BALUN CORE
BT1	BATTERY, 3. 6V
R12 R13 R14 R15 R2 R4	RES, MF, 1/8W, 1%, 1K
R5	RES, MF, 1/8W, 1%, 10
R23 R24	RES, MF, 1/8W, 1%, 1.

WAVETEK PARTS LIST

TITLE

PCA, SCRATCH PAD

REFERENCE DESIGNATORS	PART DESCRIPTION
R9	RES, MF, 1/8W, 1%, 2K
R22	RES, MF, 1/8W, 1%, 3. C
R10	RES, MF, 1/8W, 1%, 40.
R1 R3	RES, MF, 1/8W, 1%, 4. 7
R18 R19 R20 R21	RES MODULE, 10K
R7 R8	RES MODULE
R11 R16 R17	RES MODULE
CR2	DIODE
CR1	DIODE
SW1 SW2 SW3 SW4 SW5 SW6 SW7 SW8	SWITCH, PC ROTARY
U10B U11B U12B U9B	IC
U2B	CMOS, QUAD NAND S/T
U10A U17A	CMOS, S-RAM, 128x8
U9A	NMOS, S-RAM, 128x8
U5A	TTL, NAND, DUAL 4INP
U5B	TTL, OR, QUAD 2INP

WAVETEK PARTS LIST

TITLE

PCA, SCRATCH PAD

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
0101-00-0688	WVTK	0101-00-0688	1
0103-00-0688	WVTK	0103-00-0688	1
CAC03Z5U104Z050A	CORNO	1500-01-0403	9
196D226X9015KA1	SPRAG	1500-72-2601	5
196D227X9010TE4	SPRAG	1500-72-2701	1
859-0688	WVTK	1700-00-0688	1
DILB16P-108T	BURND	2100-03-0028	1
DILB-24P-108	BURND	2100-03-0029	1
2110-001	ARTWR	2100-05-0024	3
SST-1.5M	PANDT	2800-00-0003	1
103 WHITE	CALMK	2800-07-0008	2
2873000902	FARIT	3100-00-0002	3
K03B1/1AA-GT1	QE	4000-02-0006	1
RN55D-1001F	TRW	4701-03-1001	6
RN55D-1003F	TRW	4701-03-1003	1
RN55D-1211F	TRW	4701-03-1211	2

ASSEMBLY NO.	REV
1100-00-0688	K

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U6A	TTL, D-F/F, DUAL	74F74	FAIR	8000-74-7402	1
U3B	TTL, D-F/F, DUAL	74LS74	TI	8000-74-7410	1
U8A	XCVR, 8BIT TRI-ST	DP8303N	NSC	8000-83-0300	1
U1B	IC	74132	TI	8007-41-3200	1
U1A U2A U3A U4A	TTL, MUX, DATA, 1 OF 8	74LS151	TI	8007-41-5110	4
U6B U8B	TTL, MUX, QUAD, 2INP	74LS157	TI	8007-41-5710	2
U4B U7B	TTL, CNT, SYNC 4B	74LS161	SIG	8007-41-6110	2
U13B U14B U7A	TTL, BUF, OCT 3ST OUT	74LS240	TI	8007-42-4010	3
U18A	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0190	WVTK	8600-00-0190	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, SCRATCH PAD	1100-00-0688	K

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
RN55D-2001F	TRW	4701-03-2001	1
RN55D-3011F	TRW	4701-03-3011	1
RN55D-40R2F	TRW	4701-03-4029	1
RN55D-4751F	TRW	4701-03-4751	2
4310R-101-103	BOURN	4770-00-0008	4
4310R-101-682	BOURN	4770-00-0016	2
4310R-101-102	BOURN	4770-00-0022	3
1N4005	MOT	4806-01-4005	1
MBR 120	MOT	4806-02-0120	1
2300020	EECO	5107-00-0007	8
MLM339P	MOT	7000-03-3900	4
CD4093BE	RCA	8000-40-9300	1
HM-6514-9	HARR	8000-65-1400	2
MLM6810AL	MOT	8000-68-1000	1
74LS20	TI	8000-74-2010	1
74LS32	TI	8000-74-3210	1

ASSEMBLY NO.	REV
1100-00-0688	K

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE: PARTS LIST PCA, SCRATCH PAD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 859	DWG NO 1100-00-0688 REV K
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

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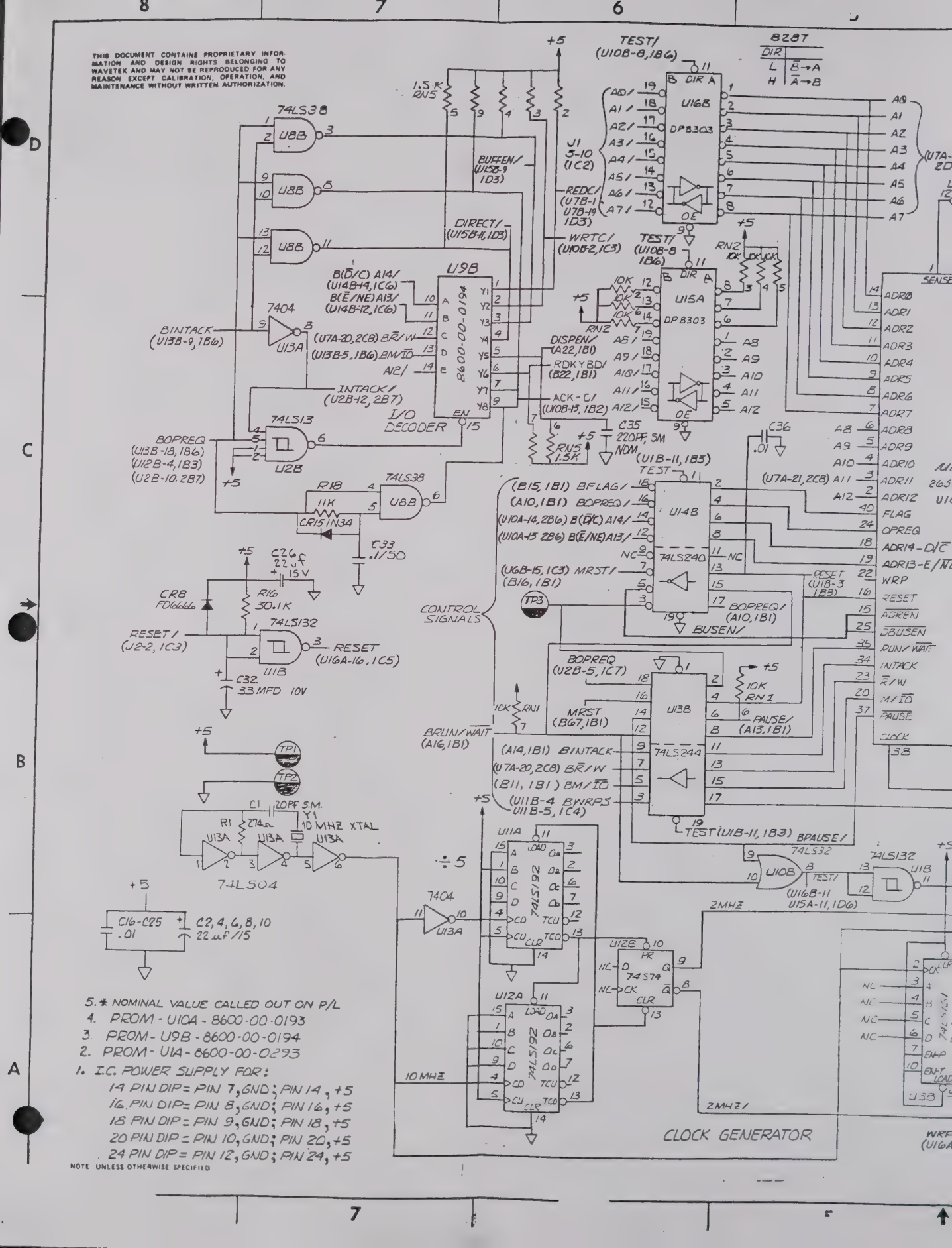
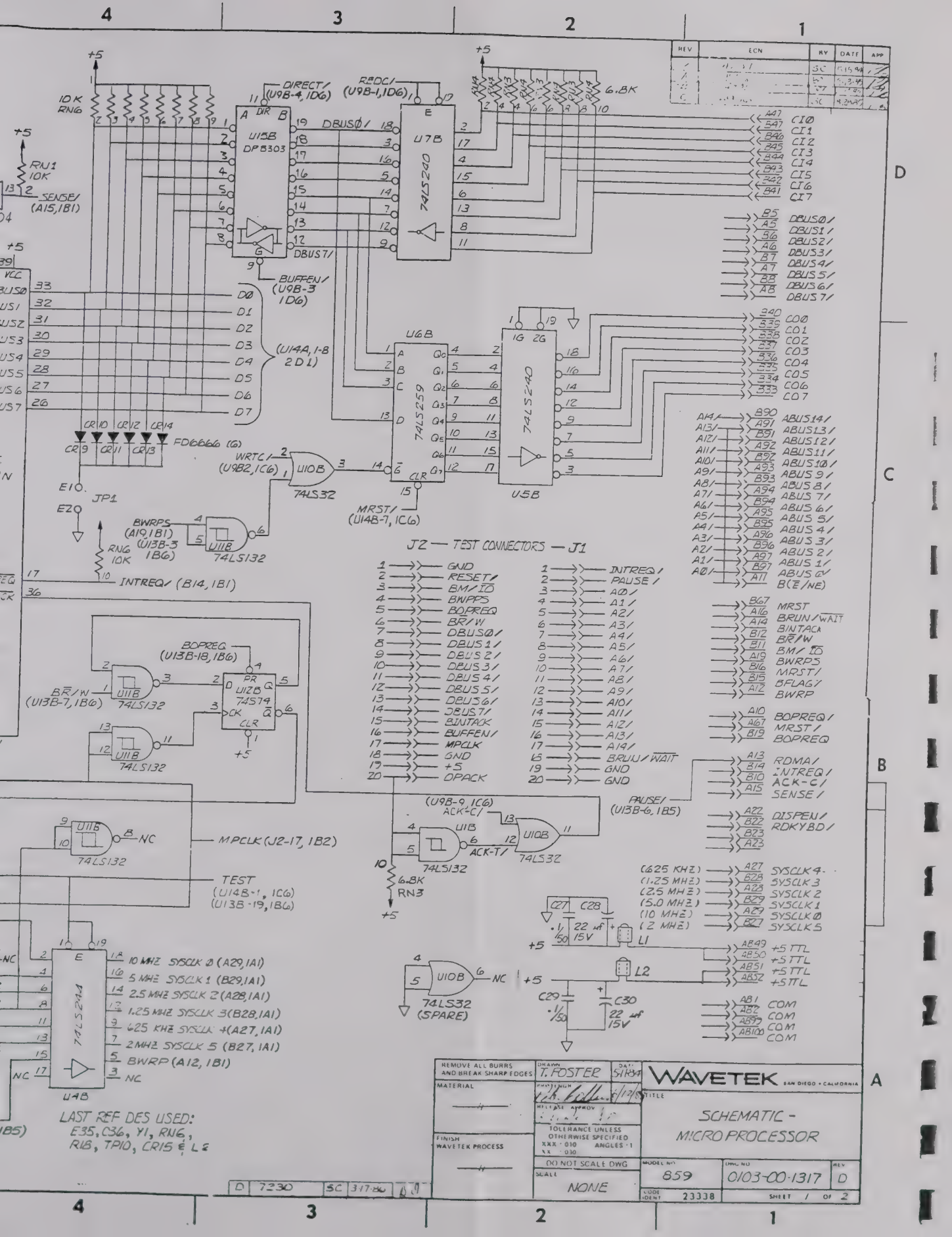


5. * NOMINAL VALUE CALLED OUT ON P/L
4. PROM - U10A - 8600-00-0193
3. PROM - U9B - 8600-00-0194
2. PROM - U1A - 8600-00-0293
1. I.C. POWER SUPPLY FOR:
   - 14 PIN DIP = PIN 7, GND; PIN 14, +5
   - 16 PIN DIP = PIN 8, GND; PIN 16, +5
   - 18 PIN DIP = PIN 9, GND; PIN 18, +5
   - 20 PIN DIP = PIN 10, GND; PIN 20, +5
   - 24 PIN DIP = PIN 12, GND; PIN 24, +5

NOTE UNLESS OTHERWISE SPECIFIED


4
3
2
1
REV
ECN
BY
DATE
APP
+5
10K RNG
DIRECT/ (U9B-4, 1D6)
RDDC/ (U9B-1, 1D6)
6.8K
U15B DP8303
U7B 74LS240
DBUS0/
DBUS7/
BUFFEN/ (U9B-3 1D6)
CI0
CI1
CI2
CI3
CI4
CI5
CI6
CI7
RN1 10K
SENSE/ (A15, 1B1)
D0
D1
D2
D3
D4
D5
D6
D7
(U14A, 1-8 2D1)
U6B 74LS259
U5B 74LS240
CO0
CO1
CO2
CO3
CO4
CO5
CO6
CO7
CR9
CR10
CR11
CR12
CR13
CR14
FD6666 (6)
WRTC/ (U9B2, 1C6)
U11B 74LS32
MRST/ (U14B-7, 1C6)
E10
E20
JP1
BWRPS (A19, 1B1) (U13B-3 1B6)
U11B 74LS132
RNG 10K
INTREQ/ (B14, 1B1)
J2 — TEST CONNECTORS — J1
GND
RESET/
BM/ IO
BWPPS
BOPREQ
BR/W
DBUS0/
DBUS1/
DBUS2/
DBUS3/
DBUS4/
DBUS5/
DBUS6/
DBUS7/
BINTACK
BUFFEN/
MPCLK
GND
+5
OPACK
INTREQ/
PAUSE/
A0/
A1/
A2/
A3/
A4/
A5/
A6/
A7/
A8/
A9/
A10/
A11/
A12/
A13/
A14/
BRUN/ WAIT
GND
GND
ABUS14/
ABUS13/
ABUS12/
ABUS11/
ABUS10/
ABUS 9/
ABUS 8/
ABUS 7/
ABUS 6/
ABUS 5/
ABUS 4/
ABUS 3/
ABUS 2/
ABUS 1/
ABUS 0/
B(E/NE)
MRST
BRUN/ WAIT
BINTACK
BR/W
BM/ IO
BWRPS
MRST/
BFLAG/
BWRP
BOPREQ/
MRST/
BOPREQ
RDMA/
INTREQ/
ACK-C/
SENSE/
DISPEN/
RDKYBD/
PAUSE/ (U13B-6, 1B5)
BOPREQ (U13B-18, 1B6)
BR/W (U13B-7, 1B6)
U11B 74LS132
U12B 74S74
+5
(U9B-9, 1C6) ACK-C/
ACK-T/
U10B 74LS32
6.8K RN3
MPCLK (J2-17, 1B2)
TEST (U14B-1, 1C6) (U13B-19, 1B6)
NC
(625 KHZ) SYSCLK 4
(1.25 MHZ) SYSCLK 3
(2.5 MHZ) SYSCLK 2
(5.0 MHZ) SYSCLK 1
(10 MHZ) SYSCLK 0
(2 MHZ) SYSCLK 5
C27 .1/50
C28 22 mf 15V
L1
L2
C29 .1/50
C30 22 mf 15V
+5 TTL
+5 TTL
+5 TTL
+5 TTL
COM
COM
COM
COM
U4B 74LS244
10 MHZ SYSCLK 0 (A29, 1A1)
5 MHZ SYSCLK 1 (B29, 1A1)
2.5 MHZ SYSCLK 2 (A28, 1A1)
1.25 MHZ SYSCLK 3 (B28, 1A1)
625 KHZ SYSCLK 4 (A27, 1A1)
2 MHZ SYSCLK 5 (B27, 1A1)
BWRP (A12, 1B1)
U10B 74LS32 (SPARE)
LAST REF DES USED: E35, C36, Y1, RN6, R18, TP10, CR15 & L2
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN T. FOSTER
DATE 5/18/84
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .030
DO NOT SCALE DWG
SCALE NONE
WAVETEK SAN DIEGO, CALIFORNIA
TITLE
SCHEMATIC - MICRO PROCESSOR
MODEL NO 859
DWG NO 0103-00-1317
REV D
CODE IDENT 23338
SHEET 1 OF 2
D 7230 SC 3-17-86

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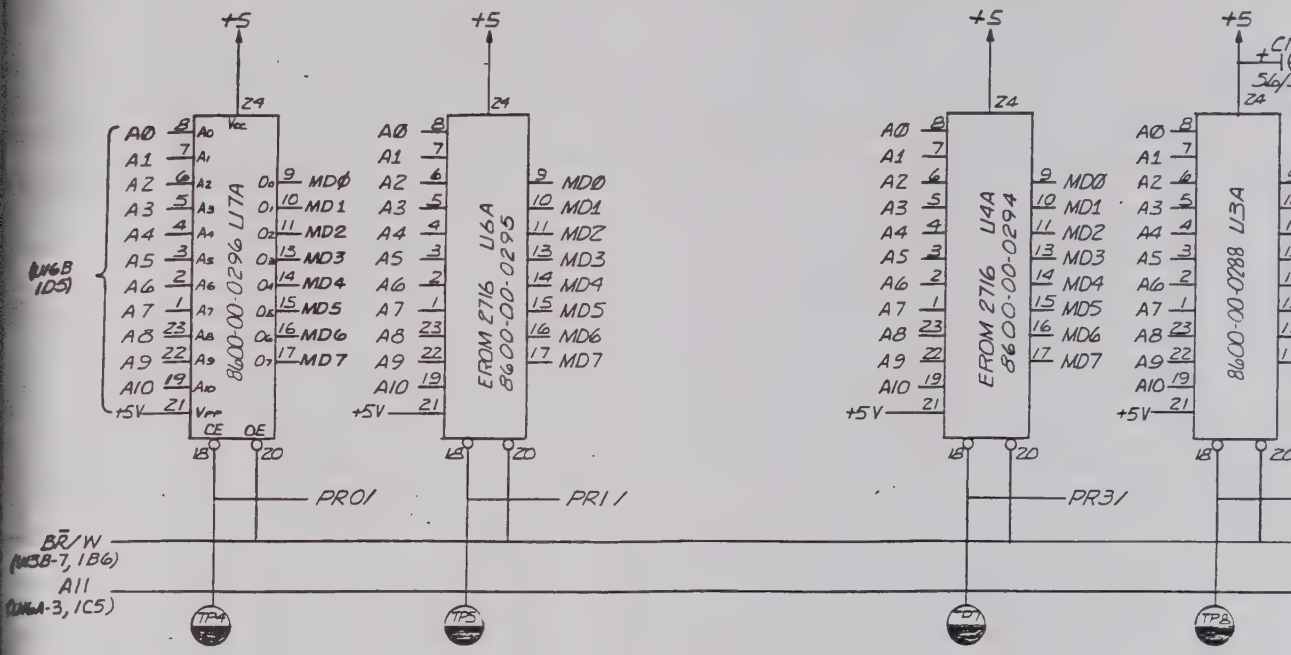
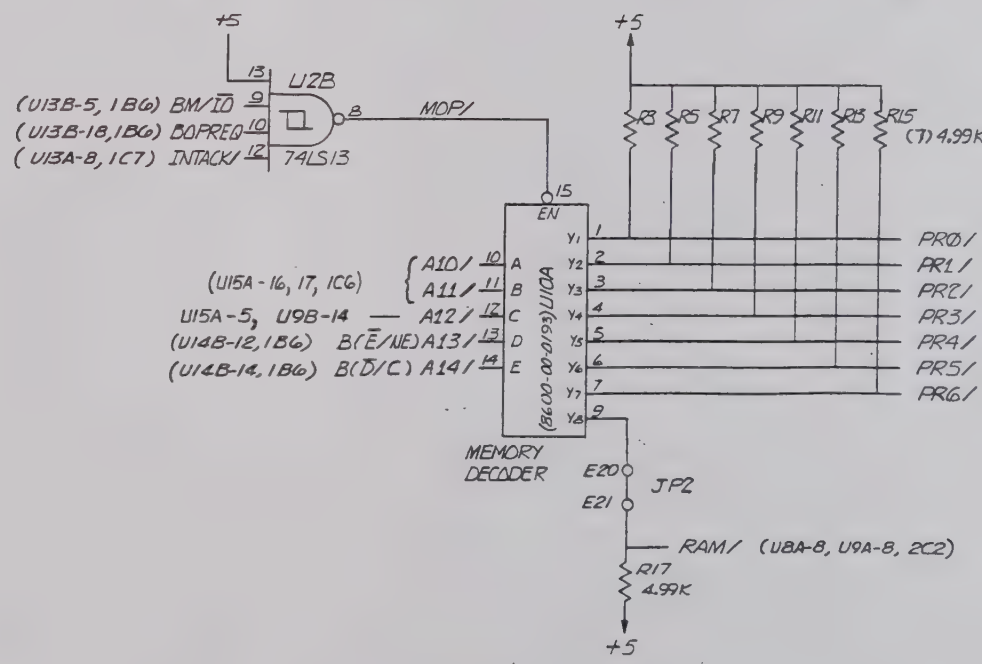
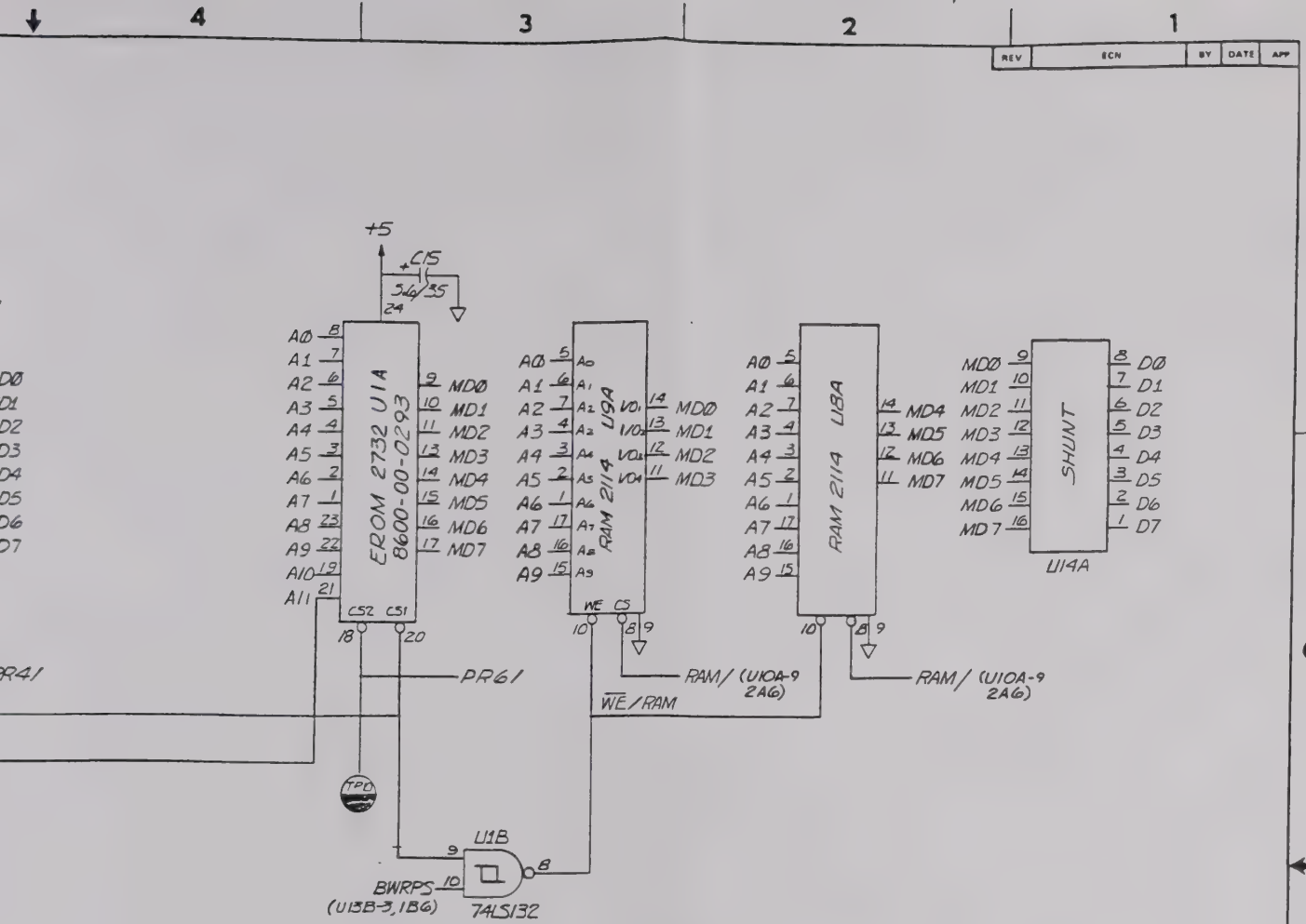




UNLESS OTHERWISE SPECIFIED



REV	ECN	BY	DATE	APP

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN T. FOSTER	DATE 51284	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	PROJENG		TITLE SCHEMATIC - MICRO PROCESSOR (EPROM MEMORY)
FINISH WAVETEK PROCESS —	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG		MODEL NO 859 / DWG NO 0103-00-1317 / REV D
	SCALE NONE		CODE IDENT 23338 / SHEET 2 OF 2

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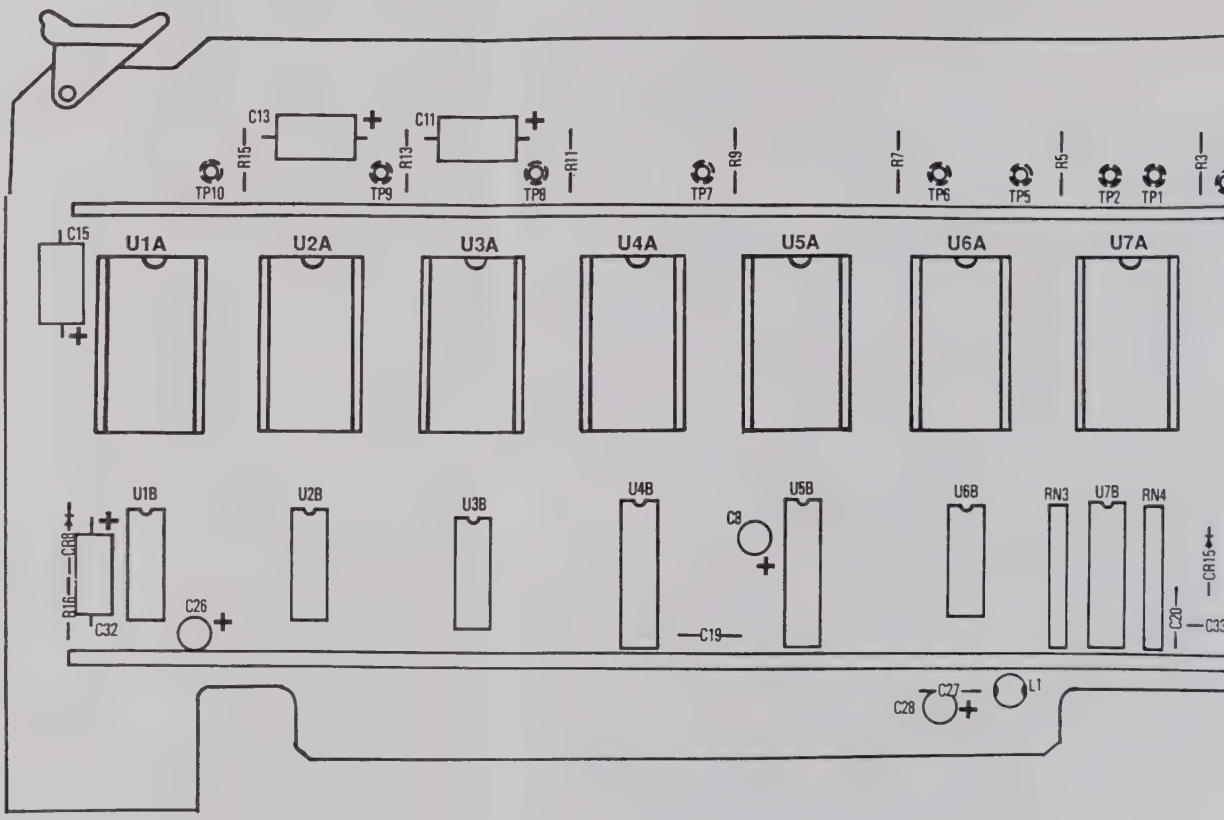

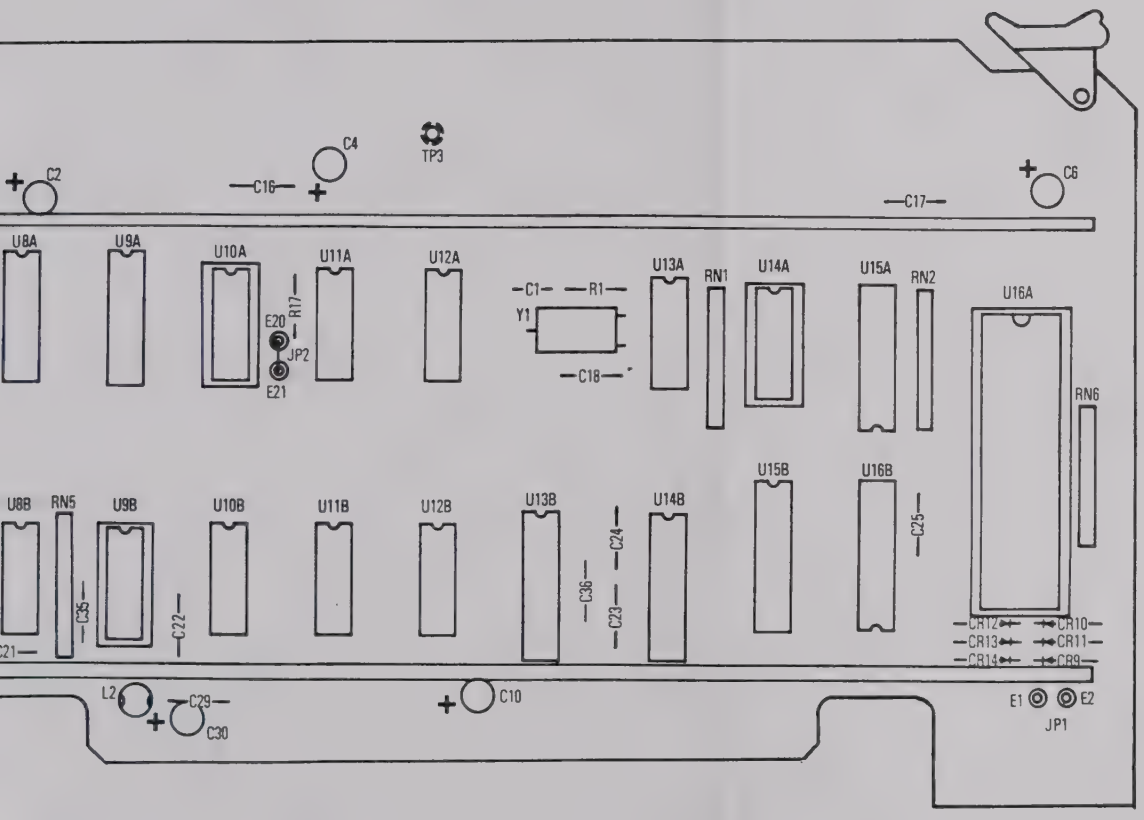

MADE FROM 0100-00-0699-3D

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROTECH-R		TITLE: MICROPROCESSOR
FINISH: WAVETEK PROCESS	RELEASE APPROV.		
	TOLERANCE UNLESS OTHERWISE SPECIFIED: XXX .010 ANGLES ± XX .030		
	DO NOT SCALE DWG		SIZE: A — DWG NO: 1100-00-1317 — REV: D
	ALT		859 — SCALE: 23338 — SHEET 1 OF 1

THIS DOCUMENT CONTAINS PROPRIETARY INFORMATION AND DESIGN RIGHTS BELONGING TO WAVETEK AND MAY NOT BE REPRODUCED FOR ANY REASON EXCEPT CALIBRATION, OPERATION, AND MAINTENANCE WITHOUT WRITTEN AUTHORIZATION.

REFERENCE DESIGNATORS	PART DESCRIPTIO
NONE	ASSY DRWG, MICR BOARD
NONE	SCHEMATIC, MICR BOARD
C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C36	CAP, CER, MN, .01M
C27 C29 C33	CAP, CER, MON, .1M
C1	CAP, MICA, 20PF, 5
C35T	CAP, MICA, 220PF,
C10 C2 C26 C28 C30 C4 C6 C8	CAP, TANT, 22MF, 1
C32	CAP, TANT, 33MF, 1
C11 C13 C15	CAP, TANT, 5.6MF,
NONE	M-PROC
NONE	SKT, IC, 16PIN
NONE	SKT, IC, 24PIN
NONE	SKT, IC, 40PIN
TP1 TP10 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	PIN, MALE
Y1	CRYSTAL, 10MHZ

WAVETEK PARTS LIST	TITLE
	PCA, MICRO, PROC

REFERENCE DESIGNATORS	PART DESCRIPTIO
NONE	PC BD EJECTOR
NONE	TRANSIPAD
U14A	SHUNT
NONE	JUMPER
NONE	PINS, JUMPER
L1 L2	BALUN CORE
R18	RES, MF, 1/8W, 1%,
R1	RES, MF, 1/8W, 1%,
R16	RES, MF, 1/8W, 1%,
R11 R13 R15 R17 R3 R5 R7 R9	RES, MF, 1/8W, 1%,
RN1 RN2 RN6	RES MODULE, 10K
RN5	RES NETWK
RN3 RN4	RES MODULE
CR15	DIODE
CR10 CR11 CR12 CR13 CR14 CR8 CR9	DIODE
NONE	POWER BUSS BAR

WAVETEK PARTS LIST	TITLE
	PCA, MICRO, PROC

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
OC	0101-00-1317	WVTK	0101-00-1317	1
OC	0103-00-1317	WVTK	0103-00-1317	1
	GE30-103ZA	MURAT	1500-01-0310	11
	CAC03Z5U104Z050A	CORNG	1500-01-0405	3
	DM15-200J	ARCO	1500-12-0000	1
	DM15-221J	ARCO	1500-12-2100	1
	196D226X9015KA1	SPRAG	1500-72-2601	8
	150D336X9010B2	SPRAG	1500-73-3601	1
	150D565X9035B2	SPRAG	1500-75-6302	3
	859-0699	WVTK	1700-00-0699	1
	DILB16P-108T	BURND	2100-03-0028	3
	DILB-24P-108	BURND	2100-03-0029	7
	DILB40P-108T	BURND	2100-03-0030	1
	60809-2	AMP	2100-05-0020	10
	590-502	WVTK	2300-99-0006	1

ASSEMBLY NO.	REV
1100-00-1317	F

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U8A U9A	MOS, RAM, 1KX4	UPD2114LC	NEC	8000-21-1400	2
U16A	IC	SCN2650AC2N40	SIG	8000-26-3001	1
U13A	IC, HEX INVERTER, LOW POWER SCHOTTKY	SN74LS04N	MOT	8000-74-0411	1
U2B	TTL, NAND, 4INP S/TRG	SN74LS13N	TI	8000-74-1310	1
U10B	TTL, OR, QUAD 2INP	74LS32	TI	8000-74-3210	1
U8B	TTL, NAND, QUAD 2INP	74LS38	TI	8000-74-3810	1
U12B	IC	74874	TI	8000-74-7401	1
U15A U15B U16B	XCVR, 8BIT TRI-ST	DP8303N	NSC	8000-83-0300	3
U11B U1B	TTL, NAND, QUAD S/TRIG	74LS132	TI	8007-41-3210	2
U3B	TTL, CNT, SYNC 4B	74LS161	SIG	8007-41-6110	1
U11A U12A	TTL, CNT, SYNC 4 UP-DN	74LS192	TI	8007-41-9210	2
U14B U5B U7B	TTL, BUF, OCT 3ST OUT	74LS240	TI	8007-42-4010	3
U13B U4B	TTL, BUF, OCT, 3 ST OUT	74LS244	TI	8007-42-4410	2
U6B	TTL, 8BIT ADDRS LTCH	SN74LS259N	TI	8007-42-5910	1
U10A	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0193	WVTK	8600-00-0193	1

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA, MICRO, PROC	1100-00-1317	F

PAGE 3

	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
	103 WHITE	CALMK	2800-07-0008	2
	10123N	METRS	2800-11-0003	1
	435704-8	AMP	3000-00-0033	1
	461-2871-01-03-10	CAMB	3000-00-0034	1
	450-3704-01-03	CAMB	3000-00-0035	4
	2873000902	FARIT	3100-00-0002	2
	RN55D-1102F	TRW	4701-03-1102	1
	RN55D-2740F	TRW	4701-03-2740	1
	RN55D-3012F	TRW	4701-03-3012	1
	RN55D-4991F	TRW	4701-03-4991	8
	4310R-101-103	BOURN	4770-00-0008	3
	785-1R1.5K	BECK	4770-00-0010	1
	4310R-101-682	BOURN	4770-00-0016	2
	1N34	FAIR	4804-01-0034	1
	1N4148	FAIR	4807-02-6666	7
	6009-90-0004	WVTK	6009-90-0004	2

ASSEMBLY NO	REV
1100-00-1317	F

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U9B	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0194	WVTK	8600-00-0194	1
U3A	IC, PROGRAMMED, REF: 8000-27-1600	8600-00-0288	WVTK	8600-00-0288	1
U1A	IC, PROGRAMMED REF: 8000-27-3200	8600-00-0293	WVTK	8600-00-0293	1
U4A	IC, PROGRAMMED REF. 8000-27-1600	8600-00-0294	WVTK	8600-00-0294	1
U6A	IC, PROGRAMMED REF: 8000-27-1600	8600-00-0295	WVTK	8600-00-0295	1
U7A	IC, PROGRAMMED REF 8000-27-1600	8600-00-0296	WVTK	8600-00-0296	1

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO	REV
PCA, MICRO, PROC	1100-00-1317	F

PAGE 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ/ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ±1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO • CALIFORNIA

TITLE

PARTS LIST
PCA, MICRO PROCESSOR

MODEL NO	DWG NO	REV
859	1100-00-1317	F
CODE IDENT 23338	SHEET 1 OF 1	

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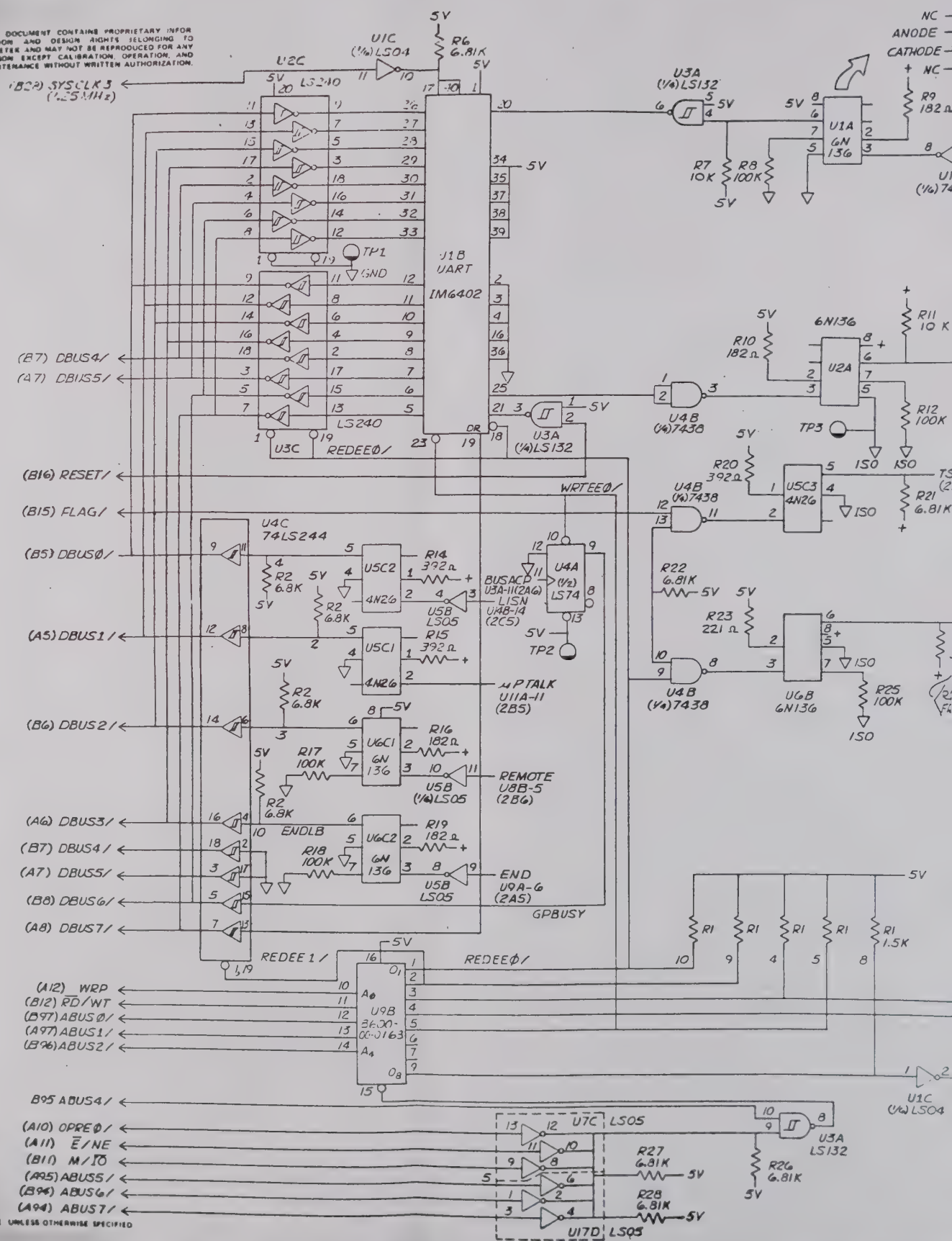
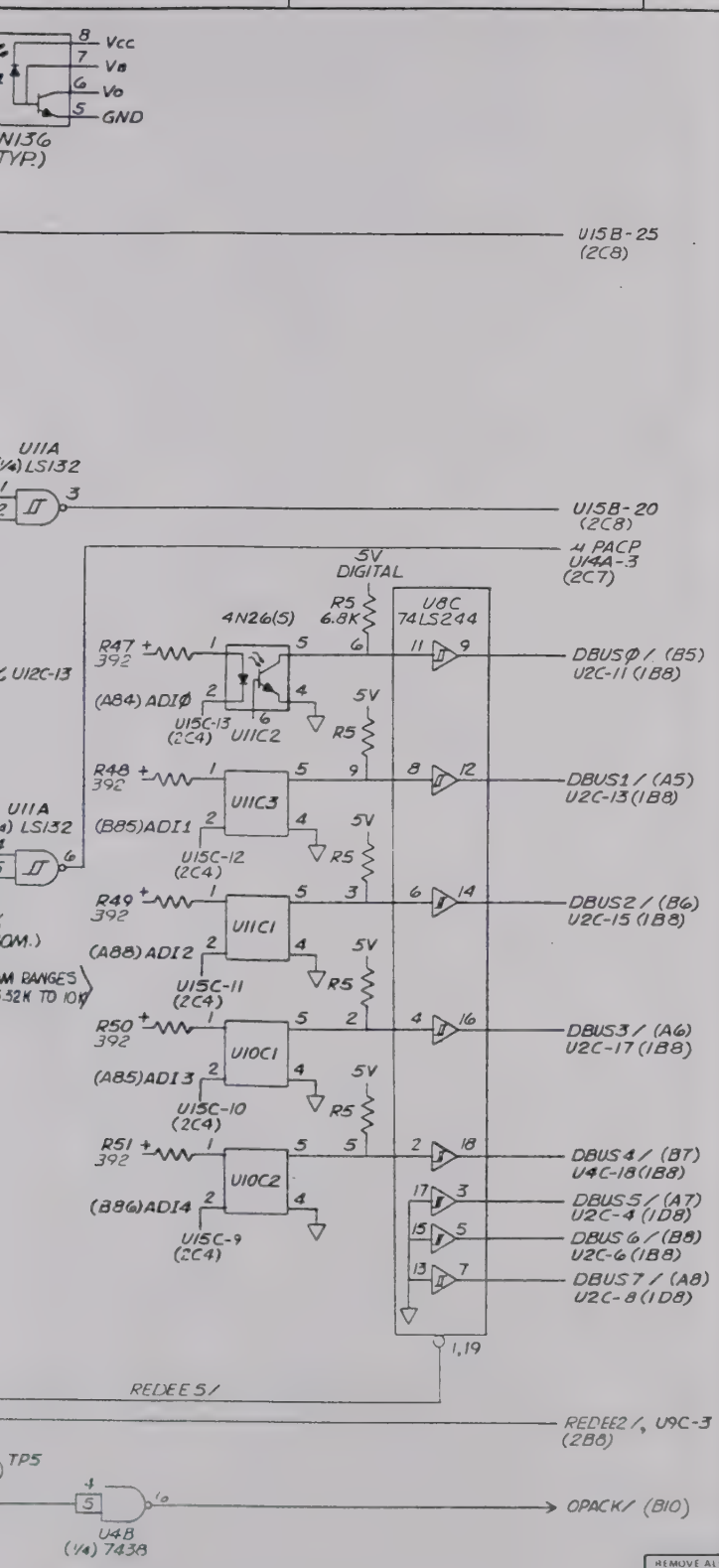
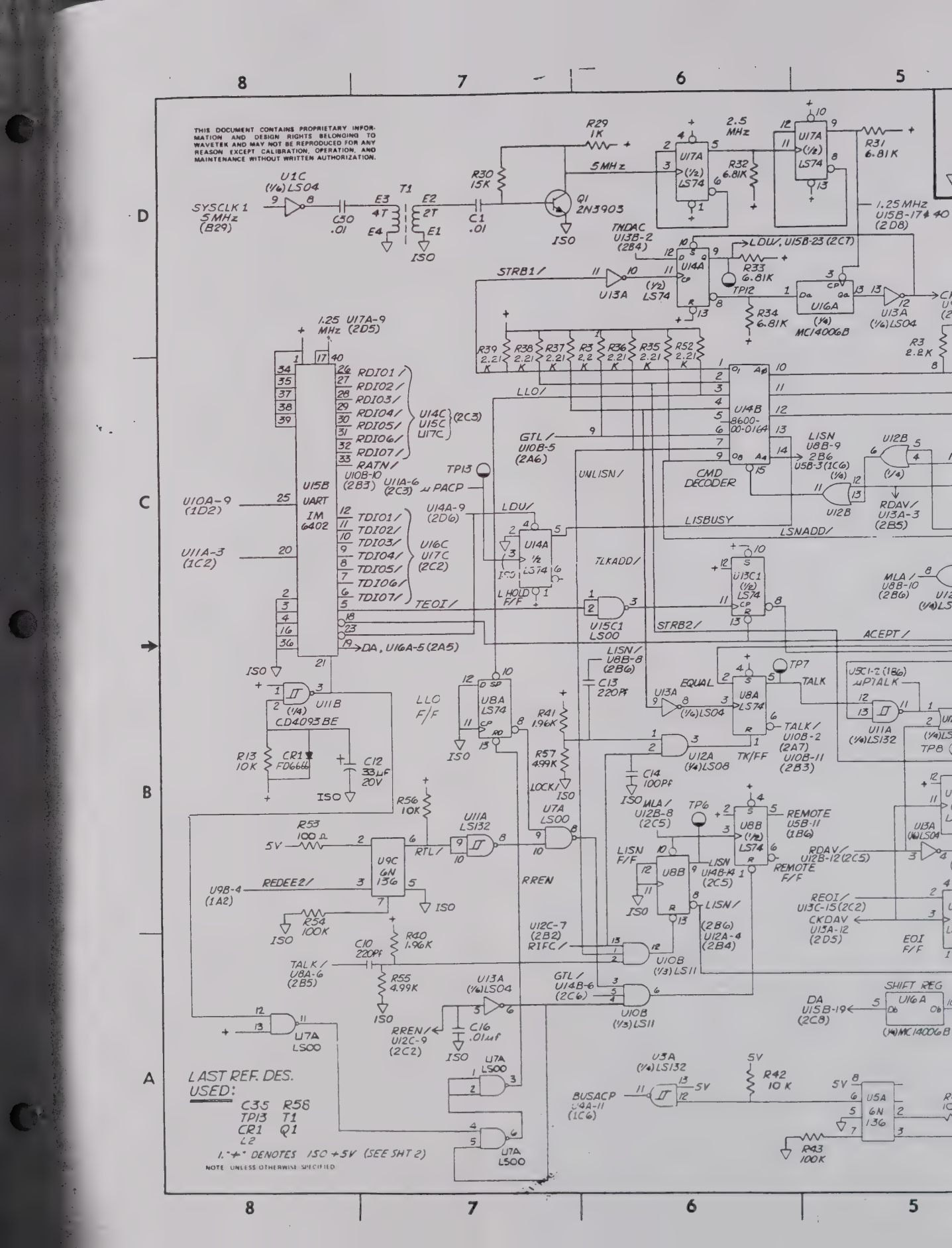




REV	ECN	BY	DATE	APP
A		L	9-4-78	
B	SNG. UPDATE	RO	2-1-79	
C	#2063	BDS	11-20-79	
D	2265, 2366	LCU	11-5-81	
E	2904		1/21/82	
F	4650	SC	1-28-85	
G	4811	SC	8-30-89	

NOTE 1. (CONT.) 5V = NORM 5V
ISO ▽ = ISO GND
▽ = NORM GND

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN D. COOPER	DATE 4-8-78	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CONCURRENCE		TITLE SCHEMATIC GPIB INTERFACE
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	SCALE	MODEL NO 859
			DWG NO 0103-00-0685 REV G
			CODE IDENT 23338 SHEET 1 OF 2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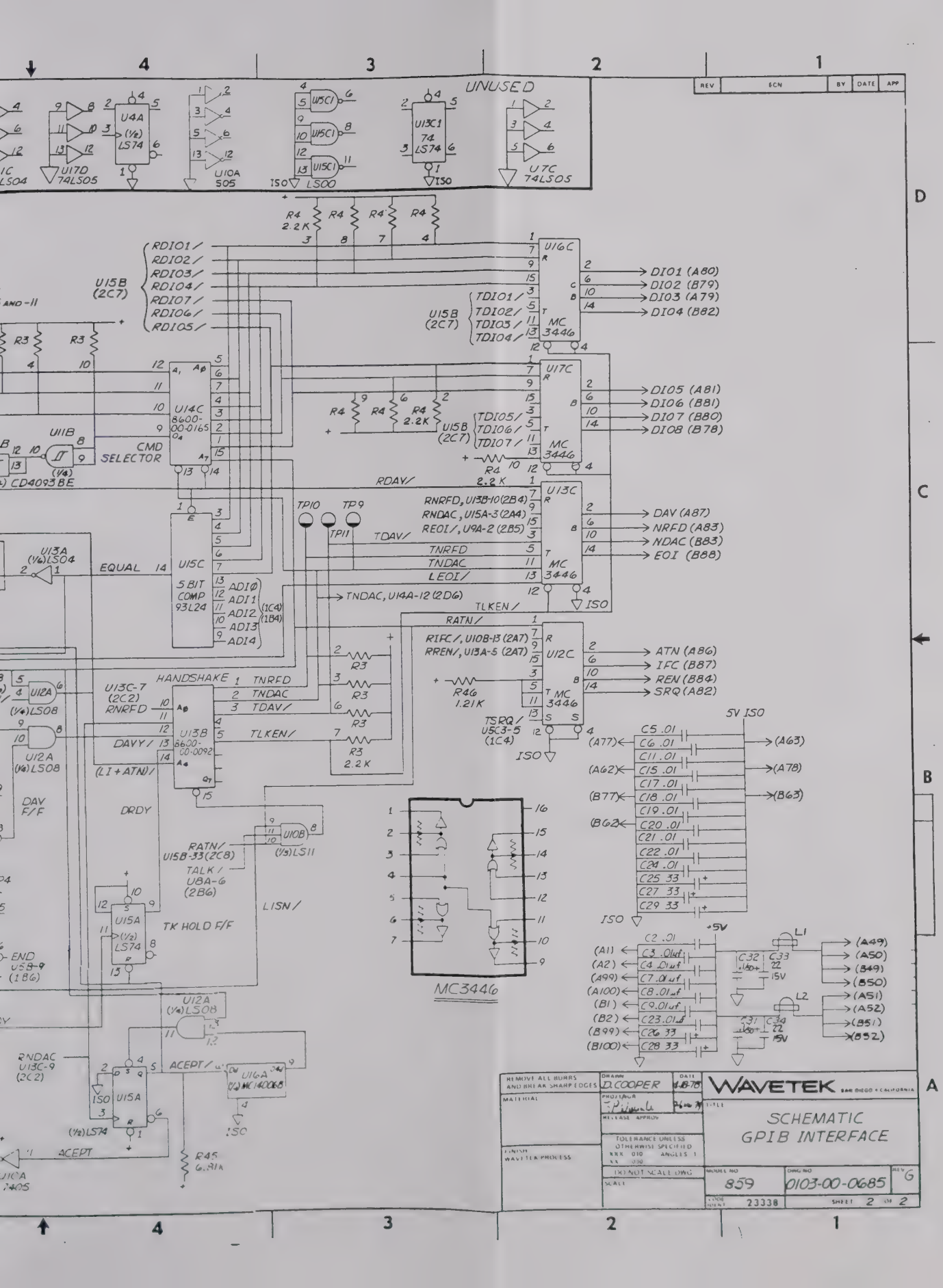
SYSCLK 1 5MHz (B29)
U1C (1/6) LS04
C30 .01
T1
E3 4T E4
E2 2T E1
C1 .01
ISO
R30 15K
Q1 2N3903
R29 1K
5MHz
2.5 MHz
U17A (1/2) LS74
R32 6.81K
R31 6.81K
1.25MHz U15B-17 & 40 (2D8)
TNDAC U13B-2 (2B4)
LDU/, U15B-23 (2C7)
U14A
R33 6.81K
STRB1/
U13A (1/2) LS74
TP12
U16A (1/4) MC14006B
R34 6.81K
U13A (1/6) LS04
1.25 MHz U17A-9 (2D5)
R39 2.21K R38 2.21K R37 2.21K R3 2.2K R36 2.21K R35 2.21K R52 2.21K
R3 2.2K
U15B UART IM 6402
RDI01/ RDI02/ RDI03/ RDI04/ RDI05/ RDI06/ RDI07/ RATN/
U14C U15C U17C (2C3)
U10B-10 (2B3)
U11A-6 (2C3)
PACP
TDI01/ TDI02/ TDI03/ TDI04/ TDI05/ TDI06/ TDI07/
U16C U17C (2C2)
TEOI/
DA, U16A-5 (2A5)
U10A-9 (1D2)
U11A-3 (1C2)
U14A-9 (2D6)
LDU/
U14A 1/2 LS74
LHOLD F/F
TP13
GTL/ U10B-5 (2A6)
UNLISN/
U14B 8600-00-0164
CMD DECODER
LISN U8B-9 2B6
U5B-3 (1C6)
U12B (1/4)
RDAV/ U13A-3 (2B5)
LISBUSY
LSNADD/
TLKADD/
U13C1 (1/2) LS74
MLA/ U8B-10 (2B6)
U15C1 LS00
STRB2/
ACEPT/
LISN/ U8B-8 (2B6)
C13 220PF
U8A LS74
EQUAL
TALK
TP7
U5C1-2 (1B6)
UNTALK
U11A (1/4) LS132
TALK/ U10B-2 (2A7)
U12A (1/4) LS08
TK/FF
U10B-11 (2B3)
TP8
U11B (1/4) CD4093BE
R13 10K
CR1 FD666
C12 33µF 20V
LLO F/F
U8A LS74
R41 1.96K
R57 4.99K
LOCK/
C14 100PF
MLA/ U12B-8 (2C5)
TP6
U8B (1/2) LS74
REMOTE U5B-11 (1B6)
REMOTE F/F
LISN F/F
U8B
LISN U14B-11 (2C5)
RDAV/ U12B-12 (2C5)
REOI/ U13C-15 (2C2)
CKDAV U13A-12 (2D5)
EOI F/F
R56 10K
R53 100Ω
5V
U11A LS132
U9C 6N 136
RTL/
U7A LS00
RREN
U9B-4 (1A2)
REDEE2/
R54 100K
C10 220PF
R40 1.96K
TALK/ U8A-6 (2B5)
R55 4.99K
U12C-7 (2B2)
RIFC/
U10B (1/3) LS11
U13A (1/6) LS04
GTL/ U14B-6 (2C6)
U10B (1/3) LS11
SHIFT REG
DA U15B-19 (2C8)
U16A (1/4) MC14006B
U7A LS00
RREN/ U12C-9 (2C2)
C16 .01µF
U7A LS00
U7A LS00
U3A (1/4) LS132
BUSACP U4A-11 (1C6)
5V
R42 10K
U5A 6N 136
R43 100K
LAST REF. DES. USED:
C35 R58
TP13 T1
CR1 Q1
L2
1. "+" DENOTES ISO +5V (SEE SHT 2)
NOTE UNLESS OTHERWISE SPECIFIED


UNUSED
U4A (1/2) LS74
U17D 74LS05
U10A 505
U15C1 LS00
U13C1 74 LS74
U7C 74LS05
U15B (2C7)
RDIO1/
RDIO2/
RDIO3/
RDIO4/
RDIO7/
RDIO6/
RDIO5/
U16C MC 3446
DIO1 (A80)
DIO2 (B79)
DIO3 (A79)
DIO4 (B82)
TDIO1/
TDIO2/
TDIO3/
TDIO4/
U17C MC 3446
DIO5 (A81)
DIO6 (B81)
DIO7 (B80)
DIO8 (B78)
TDIO5/
TDIO6/
TDIO7/
U14C 8600-00-0165
CMD SELECTOR
U11B
CD4093BE
RDAV/
U13C MC 3446
RNRFD, U13B-10 (2B4)
RNDAC, U15A-3 (2A4)
REOI/, U9A-2 (2B5)
DAV (A87)
NRFD (A83)
NDAC (B83)
EOI (B88)
TP10
TP9
TP11
TDAV/
TNRFD
TNDAC
LEOI/
TNDAC, U14A-12 (2D6)
TLKEN/
U13A (1/6) LS04
EQUAL
U15C 5 BIT COMP 93L24
ADI0
ADI1
ADI2
ADI3
ADI4
(1C4)
(1B4)
RATN/
RIFC/, U10B-13 (2A7)
RREN/, U13A-5 (2A7)
U12C MC 3446
ATN (A86)
IFC (B87)
REN (B84)
SRQ (A82)
R46 1.21K
TSRQ/ U5C3-5 (1C4)
HANDSHAKE
U13C-7 (2C2)
RNRFD
U13B 8600-00-0092
DAVY/
(LI+ATN)/
U12A (1/4) LS08
DAV F/F
DRDY
U10B (1/3) LS11
RATN/ U15B-33 (2C8)
TALK/ U8A-6 (2B6)
LISN/
U15A (1/2) LS74
TK HOLD F/F
END U5B-9 (1B6)
U12A (1/4) LS08
RNDAC U13C-9 (2C2)
ACEPT/
U16A (1/4) MC14006B
U15A (1/2) LS74
ACEPT
R45 6.81K
U10A 7405
MC3446
5V ISO
C5 .01
C6 .01
C11 .01
C15 .01
C17 .01
C18 .01
C19 .01
C20 .01
C21 .01
C22 .01
C24 .01
C25 33
C27 33
C29 33
(A77)
(A62)
(B77)
(B62)
(A63)
(A78)
(B63)
+5V
C2 .01
C3 .01uf
C4 .01uf
C7 .01uf
C8 .01uf
C9 .01uf
C23 .01uf
C26 33
C28 33
(A1)
(A2)
(A99)
(A100)
(B1)
(B2)
(B99)
(B100)
C32 1/50
C33 22 15V
C31 1/50
C34 22 15V
L1
L2
(A49)
(A50)
(B49)
(B50)
(A51)
(A52)
(B51)
(B52)
REV
ECN
BY
DATE
APP
REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN D. COOPER
DATE 4-18-78
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX .010 ANGLES 1
XX .030
DO NOT SCALE DWG
SCALE
WAVETEK SAN DIEGO • CALIFORNIA
TITLE
SCHEMATIC
GPIB INTERFACE
MODEL NO 859
DWG NO 0103-00-0685
REV G
CODE IDENT 23338
SHEET 2 OF 2

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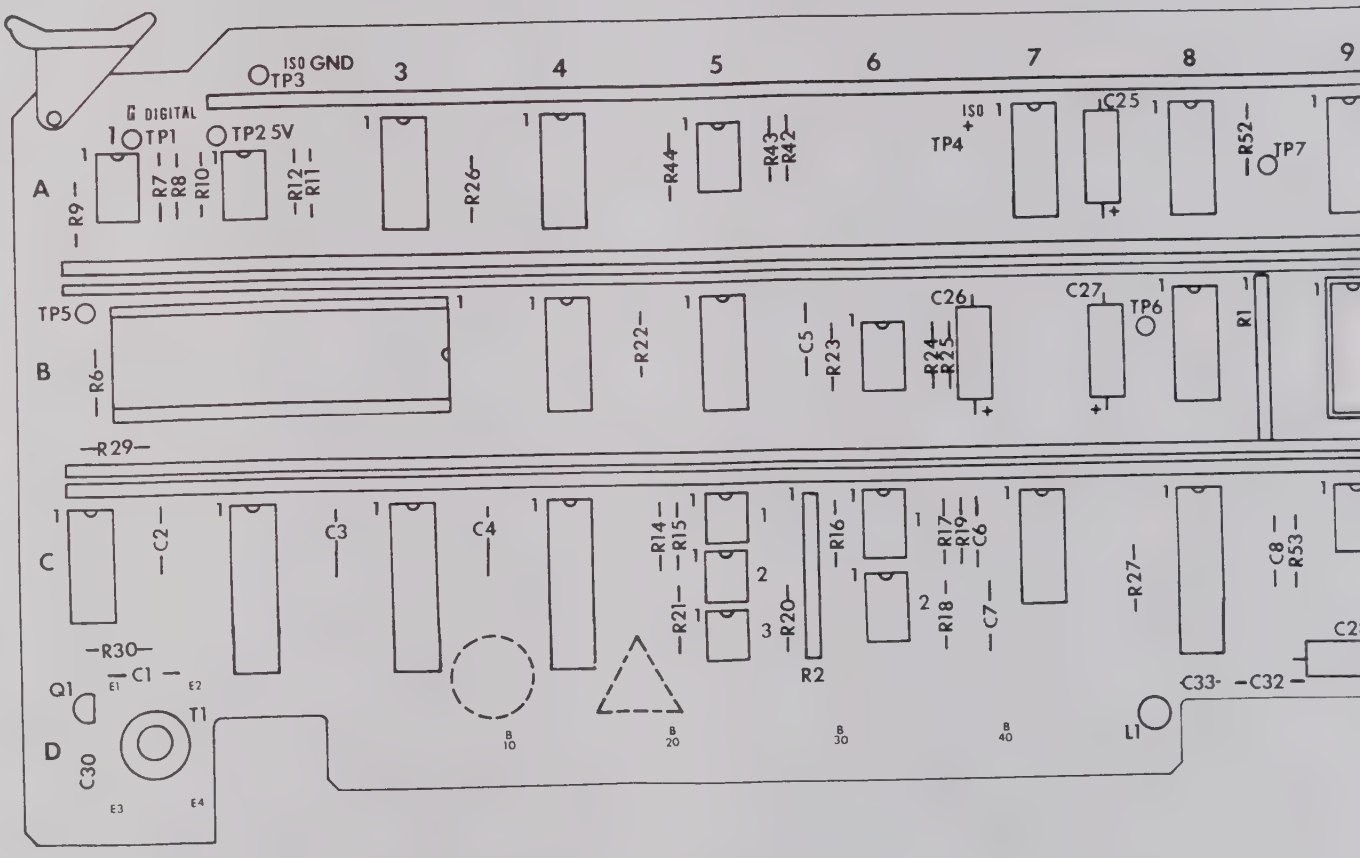

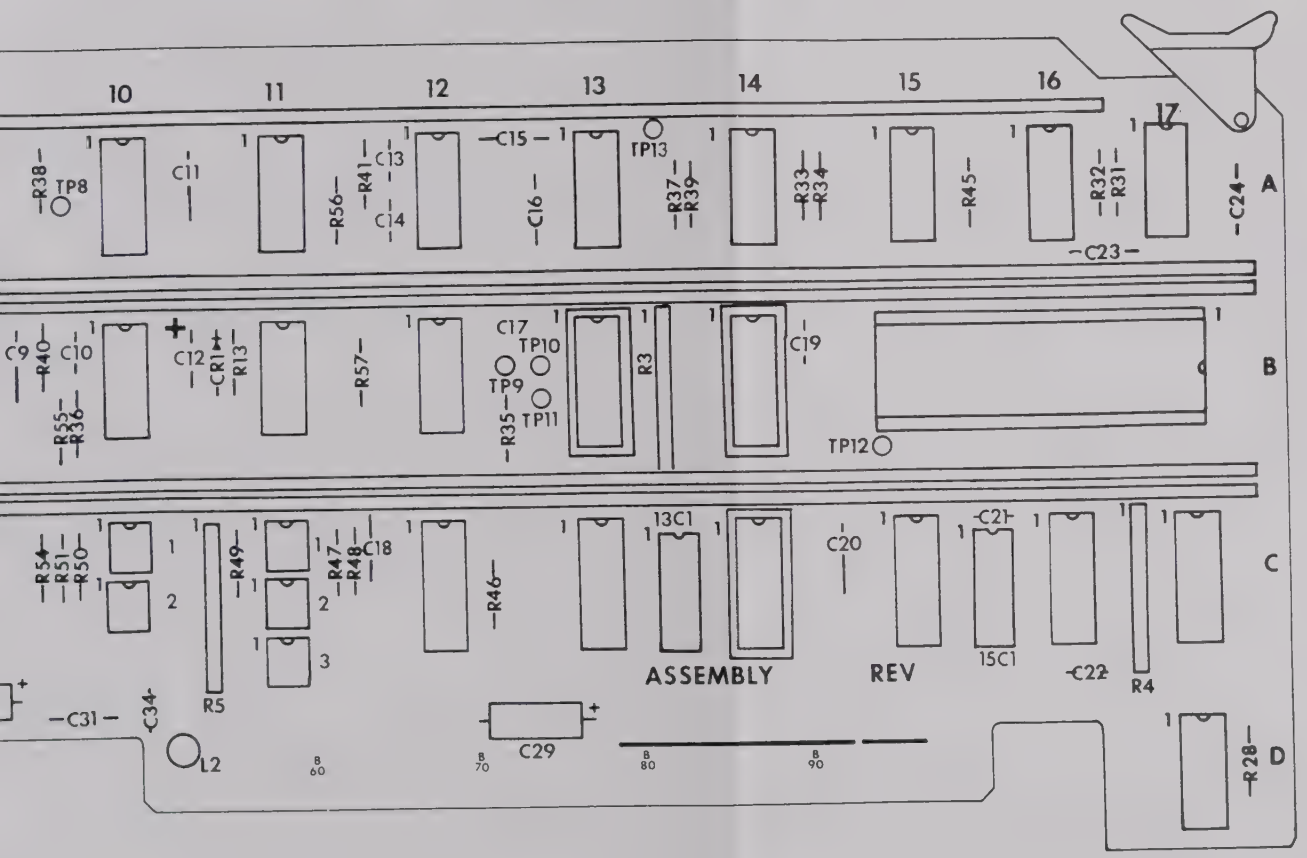

MADE FROM 0100-00-0685-3B

	WAVETEK	
MATERIAL	GPIB INTERFACE	
DO NOT SCALE DWG.	859	1100-00-0685 B
	23338	SHEET 1 OF 1

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REFERENCE DESIGNATORS	PART DESCRIPTION
NONE	ASSY DRWG INTERFA
NONE	SCHEMATIC, INTERFA
T1	TRANSFORMER
C14	CAP, CER, 100PF, 1KV
C1 C11 C15 C16 C17 C18 C19 C2 C20 C21 C22 C23 C24 C3 C30 C4 C5 C6 C7 C8 C9	CAP, CER, MN, .01MF,
C31 C32	CAP, CER, MON, 1MF,
C10 C13	CAP, CER, 220PF, 1KV
C33 C34	CAP, TANT, 22MF, 15V
C12 C25 C26 C27 C28 C29	CAP, TANT, 33MF, 10V
NONE	GPIB INTERFACE
NONE	SKT, IC, 16PIN
NONE	SKT, IC, 40PIN
TP1 TP10 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9	PIN, MALE
NONE	PC BD EJECTOR
NONE	TRANSIPAD

WAVETEK PARTS LIST

TITLE

PCA, GPIB INTERFACE

REFERENCE DESIGNATORS	PART DESCRIPTION
L1 L2	BALUN CORE
R44 R53	RES, MF, 1/8W, 1%, 10
R29	RES, MF, 1/8W, 1%, 1K
R11 R13 R42 R56 R7	RES, MF, 1/8W, 1%, 10
R12 R17 R18 R25 R43 R54 R8	RES, MF, 1/8W, 1%, 10
R46	RES, MF, 1/8W, 1%, 1.
R30	RES, MF, 1/8W, 1%, 15
R10 R16 R19 R9	RES, MF, 1/8W, 1%, 16
R40 R41	RES, MF, 1/8W, 1%, 1
R23	RES, MF, 1/8W, 1%, 22
R35 R36 R37 R38 R39 R52	RES, MF, 1/8W, 1%, 2
R24T	RES, MF, 1/8W, 1%, 3.
R14 R15 R20 R47 R48 R49 R50 R51	RES, MF, 1/8W, 1%, 3K
R55 R57	RES, MF, 1/8W, 1%, 4
R21 R22 R26 R27 R28 R31 R32 R33 R34 R45 R6	RES, MF, 1/8W, 1%, 6
R1	RES NETWK

WAVETEK PARTS LIST

TITLE

PCA, GPIB INTERFACE

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-1384

REV	ECN	BY	DATE	APP

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
0101-00-0685	WVTK	0101-00-0685	1
0103-00-0685	WVTK	0103-00-0685	1
175-0024	WVTK	1204-00-0024	1
DD-101	CRL	1500-01-0111	1
GE50-103ZA	MURAT	1500-01-0310	21
CAC03Z5U104Z050A	CORNG	1500-01-0405	2
DD-221	CRL	1500-02-2111	2
196D226X9015KA1	SPRAG	1500-72-2601	2
150D336X9010B2	SPRAG	1500-73-3601	6
172-0685	WVTK	1700-00-0685	1
DILB-16P-108	BURND	2100-03-0028	4
DILB-40P-108	BURND	2100-03-0030	2
60809-2	AMP	2100-05-0020	10
103 WHITE	CALMK	2800-07-0008	2
10123N	METRS	2800-11-0003	2

ASSEMBLY NO.	REV
1100-00-0685	

PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
R3 R4	RES MODULE 2 2K	4310R-101-222	BOURN	4770-00-0011	2
R2 R5	RES MODULE	4310R-101-682	BOURN	4770-00-0016	2
CR1	DIODE	1N4148	FAIR	4807-02-6666	1
Q1	TRANS	2N3903	NSC	4901-03-9030	1
NONE	POWER BUSS BAR (LG)	6009-90-0004	WVTK	6009-90-0004	4
NONE	POWER BUSS BAR (ST)	6009-90-0005	WVTK	6009-90-0005	1
U10C1 U10C2 U11C1 U11C2 U11C3 U3C1 U3C2 U3C3	OPTO-COUPLER	4N26	MOT	7000-04-2600	8
U1A U2A U5A U6B U6C1 U6C2 U9C	IC	6N136	SPECT	7100-00-0001	7
U12C U13C U16C U17C	IC	MC3446P	MOT	8000-34-4600	4
U11B	IC	CD4093BE	RCA	8000-40-9300	1
U15B U1B	IC	IM6402CPL	INTSL	8000-64-0200	2
U15C1 U7A	IC	74LS00	TI	8000-74-0010	2
U13A U1C	IC	74LS04	TI	8000-74-0410	2
U10A	IC	7405	TI	8000-74-0500	1
U17D U5B U7C	IC	74LS05	TI	8000-74-0510	3

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA. GPIB INTERFACE	1100-00-0685	

PAGE 3

ORIG-MFGR-PART-NO	MFGR	WAVETEK NO	QTY/PT
2873000902	FARIT	3100-00-0002	2
RN55D-1000F	TRW	4701-03-1000	2
RN55D-1001F	TRW	4701-03-1001	1
RN55D-1002F	TRW	4701-03-1002	5
RN55D-1003F	TRW	4701-03-1003	7
RN55D-1211F	TRW	4701-03-1211	1
RN55D-1502F	TRW	4701-03-1502	1
RN55D-1820F	TRW	4701-03-1820	4
RN55D-1961F	TRW	4701-03-1961	2
RN55D-2210F	TRW	4701-03-2210	1
RN55D-2211F	TRW	4701-03-2211	6
RN55D-3321F	TRW	4701-03-3321	1
RN55D-3920F	TRW	4701-03-3920	8
RN55D-4991F	TRW	4701-03-4991	2
RN55D-6811F	TRW	4701-03-6811	11
785-1R1 5%	BECK	4770-00-0010	1

ASSEMBLY NO	REV
1100-00-0685	

PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U12A	IC	74LS08	TI	8000-74-0810	1
U10B	IC	74LS11	TI	8000-74-1110	1
U12B	IC	74LS32	TI	8000-74-3210	1
U4B	IC	7438	TI	8000-74-3800	1
U13C1 U14A U15A U17A U4A U8A U8B U9A	IC	74LS74	TI	8000-74-7410	8
U15C	IC	93L24PC	FAIR	8000-93-2410	1
U16A	IC	MC14006BCP	MOT	8001-40-0600	1
U11A U3A	IC	74LS132	TI	8007-41-3210	2
U2C U3C	IC	74LS240	TI	8007-42-4010	2
U4C U8C	IC	74LS244	TI	8007-42-4410	2
U13B	IC, PROGRAMMED REF 8007-41-8801	8600-00-0092	WVTK	8600-00-0092	1
U9B	IC, PROGRAMMED REF 8007-41-8801	8600-00-0163	WVTK	8600-00-0163	1
U14B	IC, PROGRAMMED REF 8007-41-8801	8600-00-0164	WVTK	8600-00-0164	1
U14C	IC, PROGRAMMED REF 8008-21-2601	8600-00-0165	WVTK	8600-00-0165	1

WAVETEK PARTS LIST

TITLE	ASSEMBLY NO.	REV
PCA. GPIB INTERFACE	1100-00-0685	

PAGE 4

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE
MATERIAL	PROJ ENGR	
	RELEASE APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .030	
	DO NOT SCALE DWG	
	SCALE	

WAVETEK SAN DIEGO, CALIFORNIA

TITLE

PARTS LIST
PCA. GPIB INTERFACE

MODEL NO	DWG NO	REV
859	1100-00-0685	F
DOCUMENT 23338	SHEET 1 OF 1	

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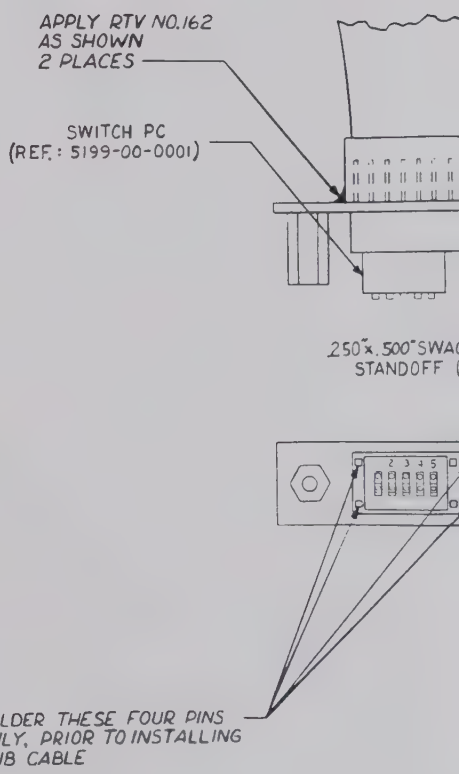

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP
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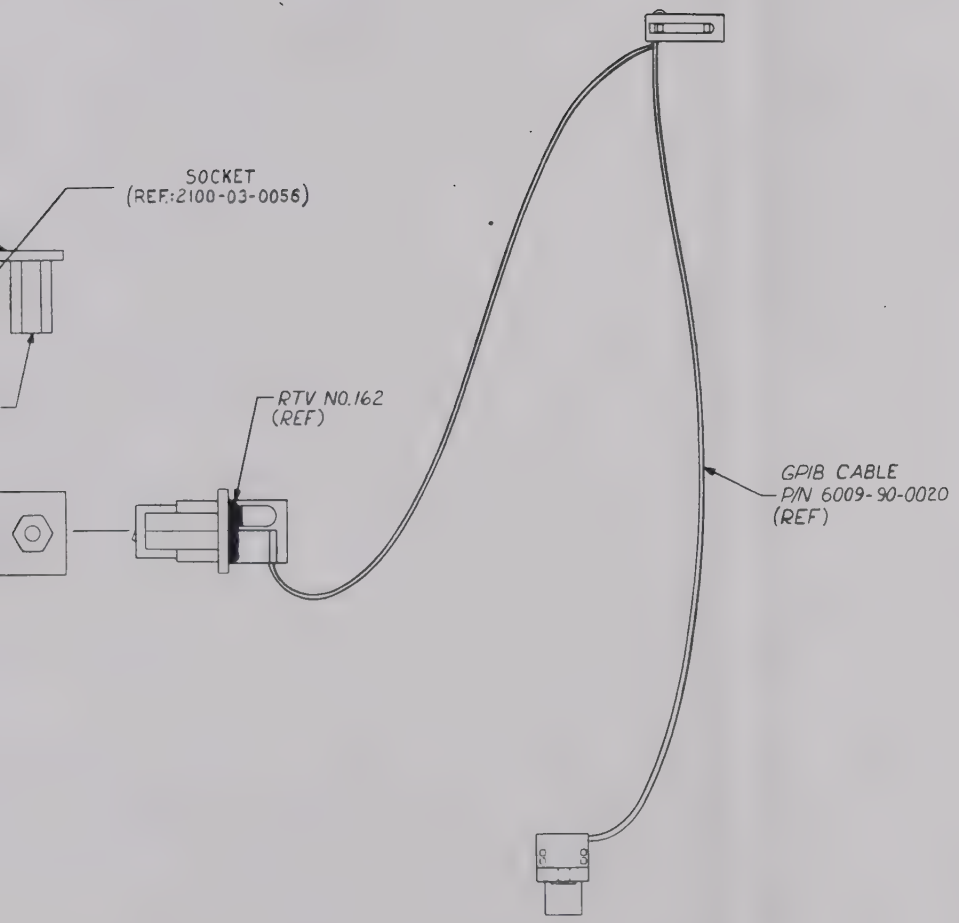


REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH
WAVETEK PROCESS

DRAWN E. REDMAN 6/14/79

PROJENGR

RELEASE APPROV
RON CONGRO 4/8/80

TOLERANCE UNLESS OTHERWISE SPECIFIED
XXX .010 ANGLES 1
XX .030

DO NOT SCALE DWG

SCALE 2/1

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
ASSEMBLY,
GPIB DECODER BD

MODEL NO

DWG NO 0101-00-0730 REV A

23338 SHEET 1 OF 1

APPENDIX A

Table A-1. American Standard Code for Information Interchange (ASCII)

b7 / b6 / b5 / BITS[2]					$^{0}0_{0}$	MSG[1]	$^{0}0_{1}$	MSG	$^{0}1_{0}$	MSG	$^{0}1_{1}$	MSG	$^{1}0_{0}$	MSG	$^{1}0_{1}$	MSG	$^{1}1_{0}$	MSG	$^{1}1_{1}$	MSG
b4	b3	b2	b1	column / row	0		1		2		3		4		5		6		7	
0	0	0	0	0	NUL		DLE		SP	MLA ASSIGNED TO DEVICE	0	MLA ASSIGNED TO DEVICE	@	MTA ASSIGNED TO DEVICE	P	MTA ASSIGNED TO DEVICE	\	MEANING DEFINED BY PCG CODE	p	MEANING DEFINED BY PCG CODE
0	0	0	1	1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0	0	1	0	2	STX		DC2		"		2		B		R		b		r	
0	0	1	1	3	ETX		DC3		#		3		C		S		c		s	
0	1	0	0	4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0	1	0	1	5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0	1	1	0	6	ACK		SYN		&		6		F		V		f		v	
0	1	1	1	7	BEL		ETB		'		7		G		W		g		w	
1	0	0	0	8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1	0	0	1	9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1	0	1	0	10	LF		SUB		*		:		J		Z		j		z	
1	0	1	1	11	VT		ESC		+		;		K		[		k		{	
1	1	0	0	12	FF		FS		,		<		L		\		l		¦	
1	1	0	1	13	CR		GS		-		=		M		]		m		}	
1	1	1	0	14	SO		RS		.		>		N		^		n		~	
1	1	1	1	15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear	Universal Command Group
DC1	=	LLO	Local lockout	
NAK	=	PPU	Parallel poll unconfigure	
EM	=	SPD	Serial poll disable	
CAN	=	SPE	Serial poll enable	
SOH	=	GTL	Go to local	Addressed Command Group
EOT	=	SDC	Selected device clear	
ENQ	=	PPC	Parallel poll configure	
BS	=	GET	Group execute trigger	
HT	=	TCT	Take control	

APPENDIX B

Table B-1. Programming Command Summary (Excluding GPIB Command Groups, which are given in Appendix A)

Control and Data Names	Model 859 Key	ASCII Character
Change Signs	+/–	–
Decimal Point	.	.
0,1,2, . . . 9	0,1,2, . . . 9	0,1,2, . . . 9
Upper Amplitude	LEVEL UPPER	A
Mode	MODE	B
Function	FUNC	C
Lower Amplitude	LEVEL LOWER	D
×10 Multiplier	EXP	E
Frequency	REPETITION FREQ	F
Output Channel	CHNL	G
Gate Reset	MAN TRIG (Release)	H
Execute	EXEC	I
Manual Trigger	MAN TRIG (Push)	J
Trigger Format	TRIG FORMT	K
Delay	DELAY	L
Store Settings	STORE SET	M
Width	WIDTH	N
Output Normal or Complemented	OUTPUT NORM/COMP	O
Output Off or On	OUTPUT OFF/ON	P
Burst Length	BURST	R
Period	REPETITION PER	S
Recall Next Stored Setting	None	T
Leading Edge	TRANSITION LEAD EDGE	U
Trailing Edge	TRANSITION TRAIL EDGE	V
Time Interval	TIME INTVL	W
Recall Previous Stored Setting	None	X
Recall Stored Setting	RCL SET	Y
System Reset	RESET	Z
GET	None	%G
Service Request	None	%Q
Talk Message	None	%T
Terminator Select	None	%X

Function (C) Codes

0	Single Pulse
1	Double Pulse
2	Square Wave
3	Inhibit (no output, no error checking)

Mode (B) Codes

0	Continuous
1	Triggered
2	Gated
3	Burst
4	External Width
5	Time Interval

Table B-1. Programming Command Summary (Continued)

Trigger Format (K) Codes	
0	BNC Rear Panel Connector, Rising Edge
1	BNC Rear Panel Connector, Falling Edge
2	Manual Trigger From Front Panel or GPIB

Output Off/On (P) Codes	
0	Off
1	On

Talk Message (%T) Codes	
	NOTE *This parameter selects which kind of message the 859 will send when it is addressed as a talker on the GPIB.*
0	Status of triggered indicator. H 1 is sent if the instrument is outputting a waveform in the triggered, burst or time interval mode. H 0 is sent if not.
1	List of action and parameter selectors which caused programming errors. When read, this list is set to null.
2	Poll byte which would be sent in response to a GPIB serial poll.
3	Value of parameter selected by the most recently programmed selector.
4	State of waveform parameters common to both channels.
5	State of waveform parameters in channel 1.
6	State of waveform parameters in channel 2.

Output Normal/Complemented (O) Codes	
0	Normal
1	Complemented

SRQ (%Q) Codes	
	NOTE *This parameter selects the conditions under which the GPIB SRQ signal will be sent by the 859.*
0	SRQ not sent
1	SRQ sent if a programming error occurred
2	SRQ sent upon completion of a waveform output in any mode except continuous.
3	SRQ sent if either of the events (1, 2) above occurs

Get Mode (%G) Codes	
	NOTE *This parameter selects which kind of action the 859 will take when it receives a GET command.*
0	Execute and trigger upon receipt of GET command (no error checking).
1	Fetch next stored setting, execute and trigger upon receipt of GET command (no error checking).
-1	Fetch previous stored setting, execute and trigger upon receipt of GET command (no error checking).

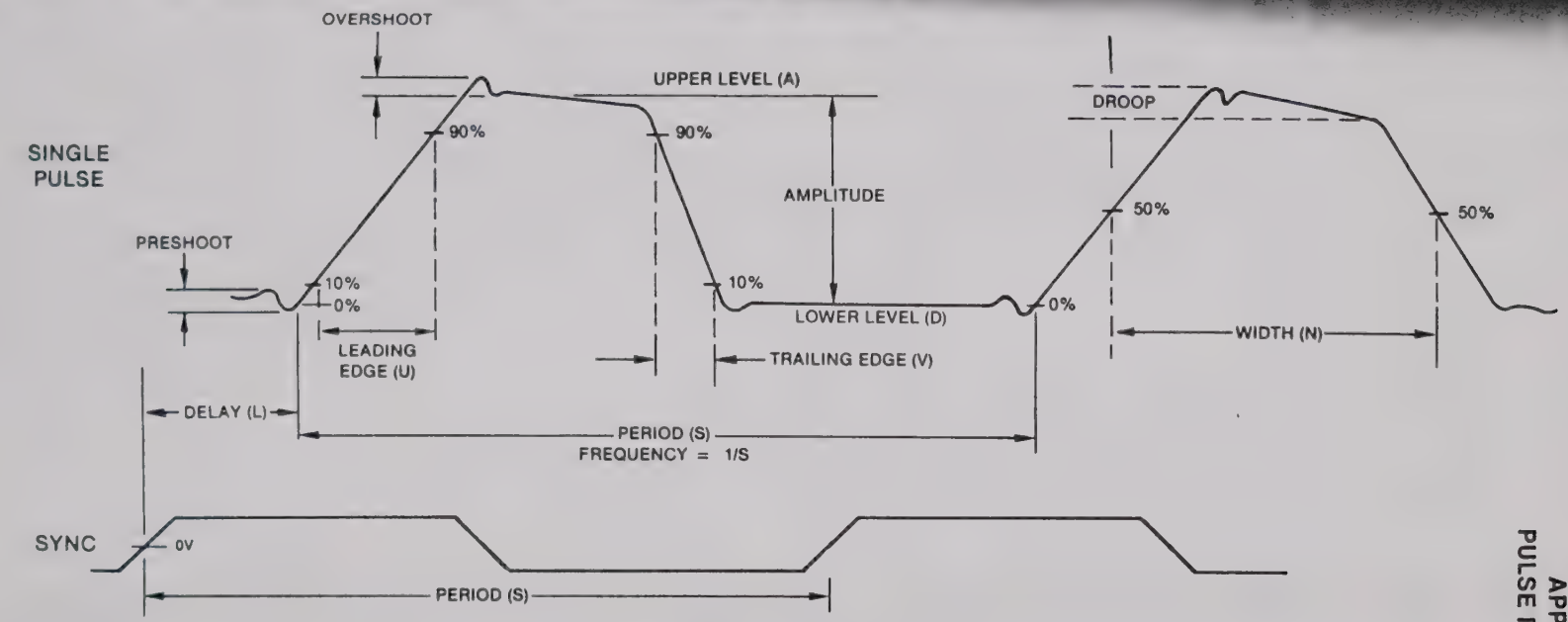


Figure C-1. Single Pulse

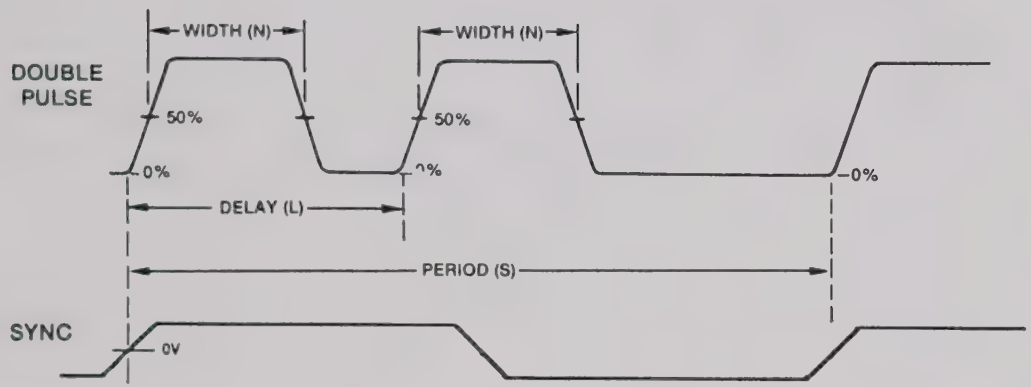


Figure C-2. Double Pulse

1. Remove top and bottom covers.

2. Add 24 gauge sleeved jumper on bottom of Mother board (1100-00-2203) from J6-B49 to J4-A49

3. Replace bottom cover.

4. Remove Burst board (grn. ejectors - 1100-00-0687) and modify per print 0101-00-0994.

5. Build 1100-00-0995 board per print 0101-00-0995.

6. Install wires on 1100-00-0995 board per print 0101-00-0995.

7. Mount onto burst board using 4-40x3/8" pan head screws and shoulder washer as per print 0101-00-0994.

8. Hook up wires as per print 0101-00-0994.

9. Remove Delay/Width board (yellow ejectors - 1100-00-0694) and modify per print 0101-00-0694-1.

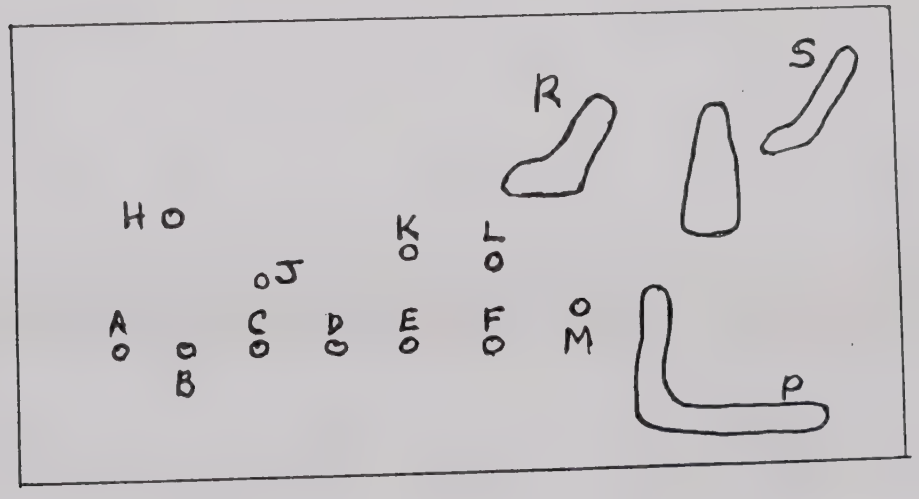
10. Modify Rear panel 1101-00-0672 per instructions, prints, and drawing 0101-00-0672-1 in folder.

11. Make sure all revised boards are marked 859-S-777 and all wires are hooked back up.

12. Put new serial tag to reflect S-777 and submit to calib.

859-S-777

CORCOM WIRING

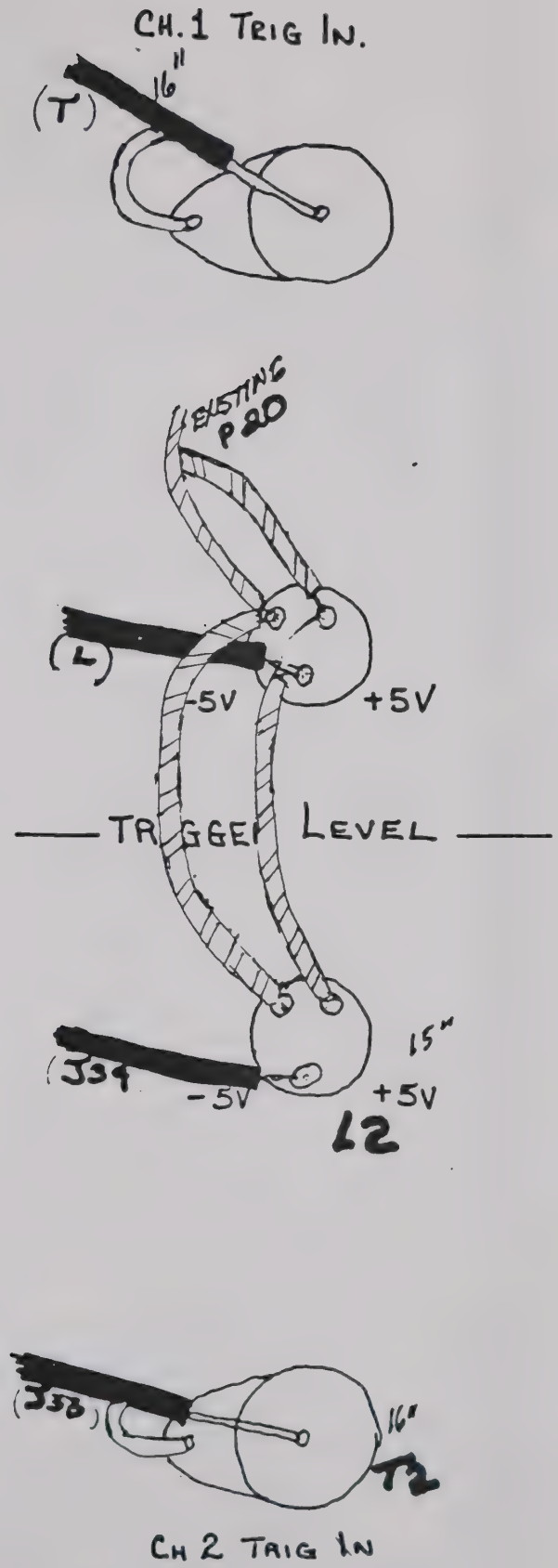


ADD RED WIRE TO J 22 GAUGE

ADD BLACK WIRE TO K 22 GAUGE

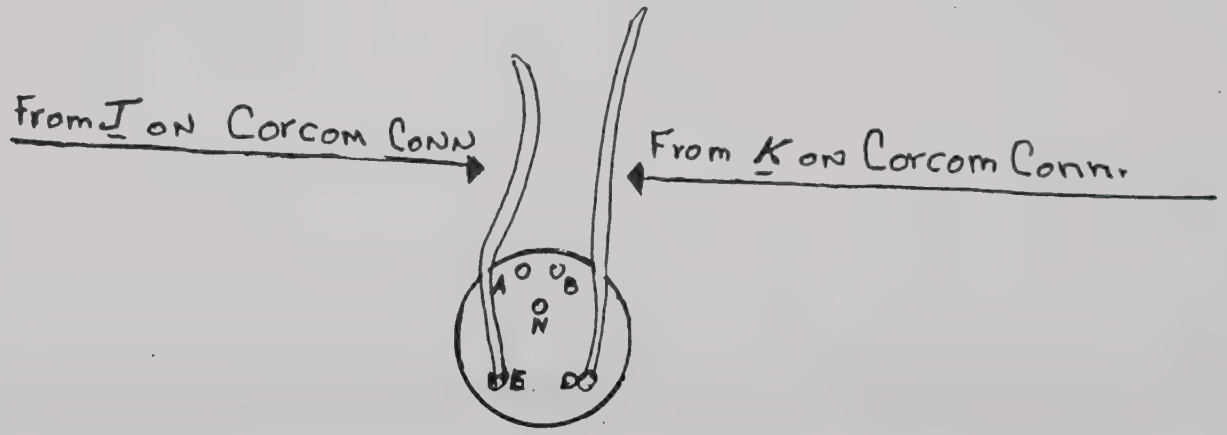
BLACK WIRE GOES TO D ON 5 PIN CONN.

RED WIRE GOES TO E ON 5 PIN CONN.


CH. 1 TRIG IN.
16"
(T)
EXISTING P20
(L)
-5V
+5V
TRIGGER LEVEL
15"
(J34
-5V
+5V
L2
(J33)
16"
T2
CH 2 TRIG IN

859-S-777

Five Pin Socket



859-S-777

1100-00-0995

REF. DESIG.	DECRIPTION	P/N	QTY.
C2, C3, C4	Cap, Ceramic, .1uf, 50V	1500-01-0504	3
C6	Cap, Tant., 22uf, 15V	1500-72-2601	1
FB1	Balun Core	3100-00-0002	1
Z1	Printed Circuit Bd.	Unique-DNP	1
R1	Res, MF, 1%, 1/8W 3.01K	4701-03-3011	1
R2, R9	Res, MF, 1%, 1/8W 1K	4701-03-1001	2
R3	Res, MF, 1%, 1/8W 7.50K	4701-03-7501	1
R4, R5, R8	Res, MF, 1%, 1/8W 100	4701-03-1000	3
R6, R7, R10, R11	Res, MF, 1%, 1/8W 78.7	4701-03-7879	4
R12	Res, MF, 1%, 1/8W 2K	4701-03-2001	1
CR1, CR2, CR3	Diode, Signal FD777	4807-02-0777	3
CR4, CR5	Diode, Signal IN4148	4807-02-6666	2
U1	I.C. MC10116P	8001-01-1600	1
U2	I.C. MC10102P	8001-01-0200	1
U3	I.C. MC10100	Unique-DNP	1
J33, J34	Jack, Conn. 27-848	2100-07-0011	2
	Spacer, Nylon 13SP162	2800-04-0013	3
	Spacer, Swedge, Standoff	2800-03-0008	3
C1	Cap, Ceramic 10pf	1500-01-0011	1
	SKT IC	2100-03-0028	1

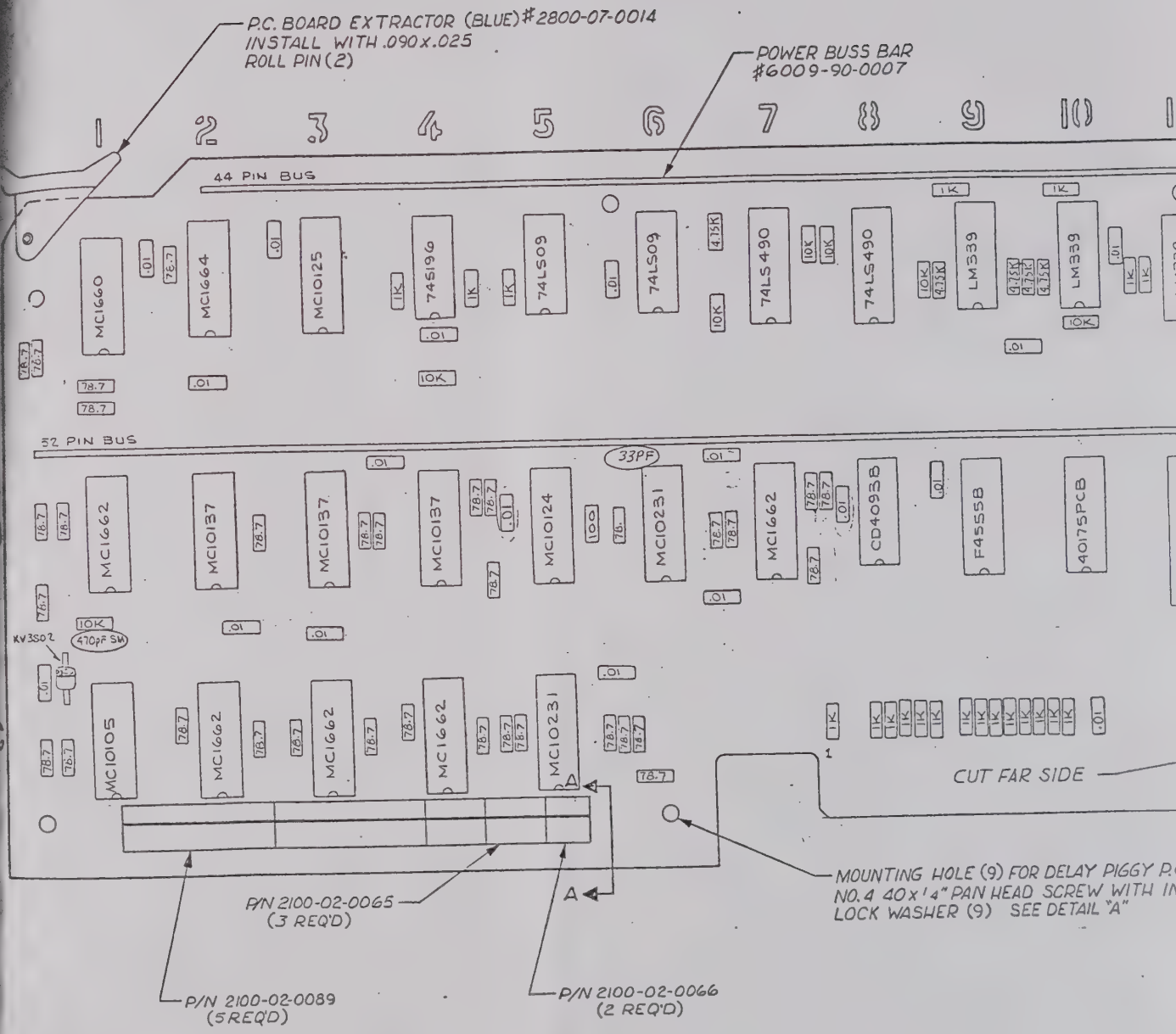
859-S-777

1101-00-0672-1

REF. DESIG.	DECRIPTION	P/N	QTY.
J32	BNC Conn. UG657/U	2100-01-0003	1
	Solder Lug 1497	2100-04-0012	1
	Shoulder Washer 2668	2800-27-0004	1
	Nylon Flat Washer	2800-28-0005	1
	Pot 5K Lock ADJ	4600-05-0209	1
R2	Butch Plug	2800-35-0001	1
	Cable Clamp	2800-00-0016	1
	Connector M5SLSN Winch.	Unique-DNP	1
	Connector M5PLSN Winch.	Unique-DNP	1
	Hood HG9C Winch.	Unique-DNP	1
	Nomenclature Plate WVK	Unique-DNP	1
	Ty-Wrap	2800-00-0003	
	Pin, Male Molex	DNP	2
	Pin, Female Molex	DNP	2

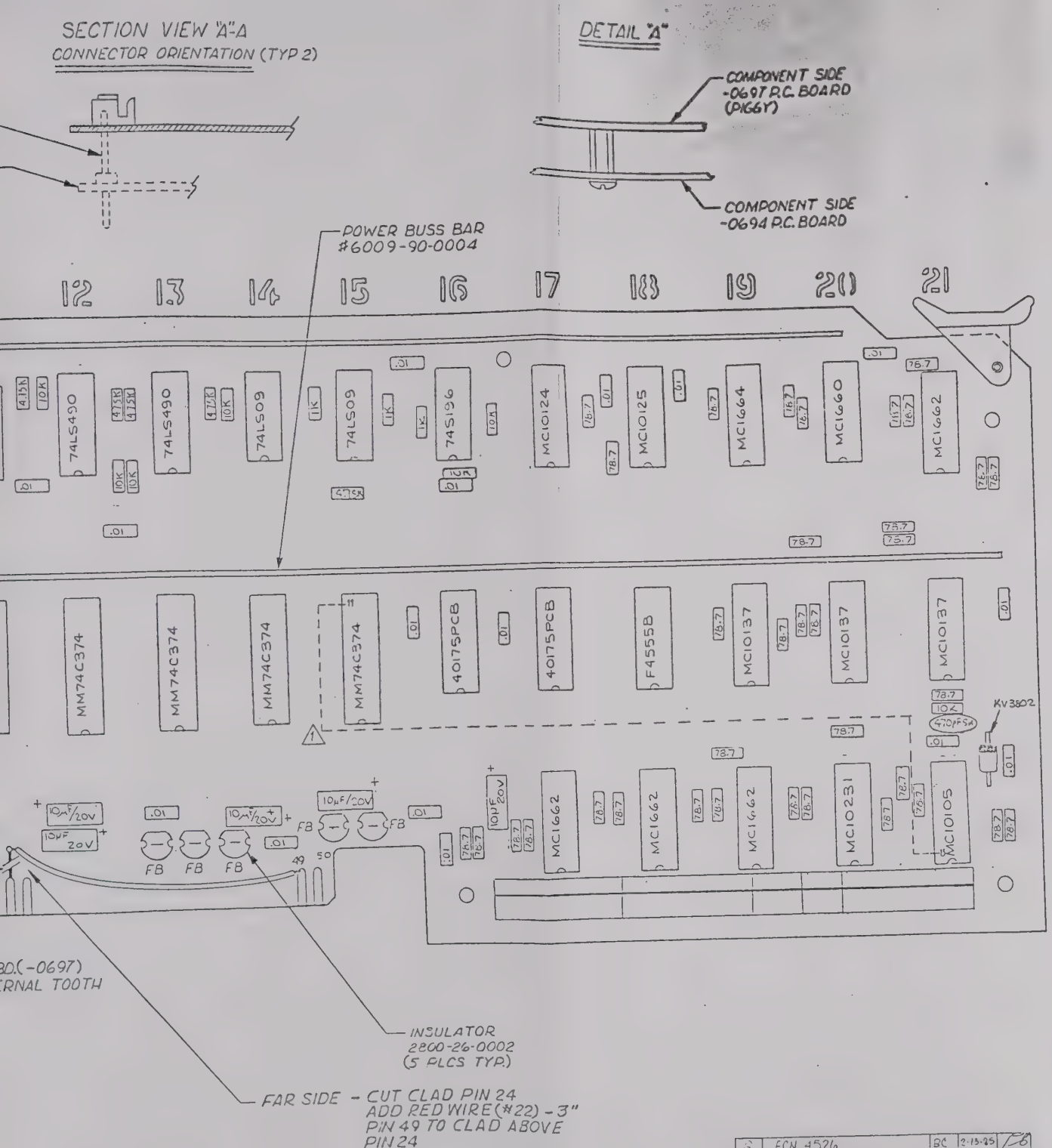
PIN ALIGNMENT –

PIGGY BOARD (RE



⚠ ON CIRCUIT SIDE, ADD JUMPER FROM U15B-11 TO U21C-13.

NOTES: UNLESS OTHERWISE SPECIFIED.



REV	ECN	BY	DATE	APP
G	ECN 4526	BC	2-13-85	[illegible]
F	ECN 4192	RO	4/23/84	[illegible]
E	3338 (CL III)	[illegible]	9/16/82	[illegible]
E	2749	[illegible]	[illegible]	[illegible]
D	UPDATED FOR REV "D" BRD	SC	4/25/80	[illegible]

ASSEMBLY
DELAY/WIDTH
BOARD

859-S-777 0101-00-0694-1

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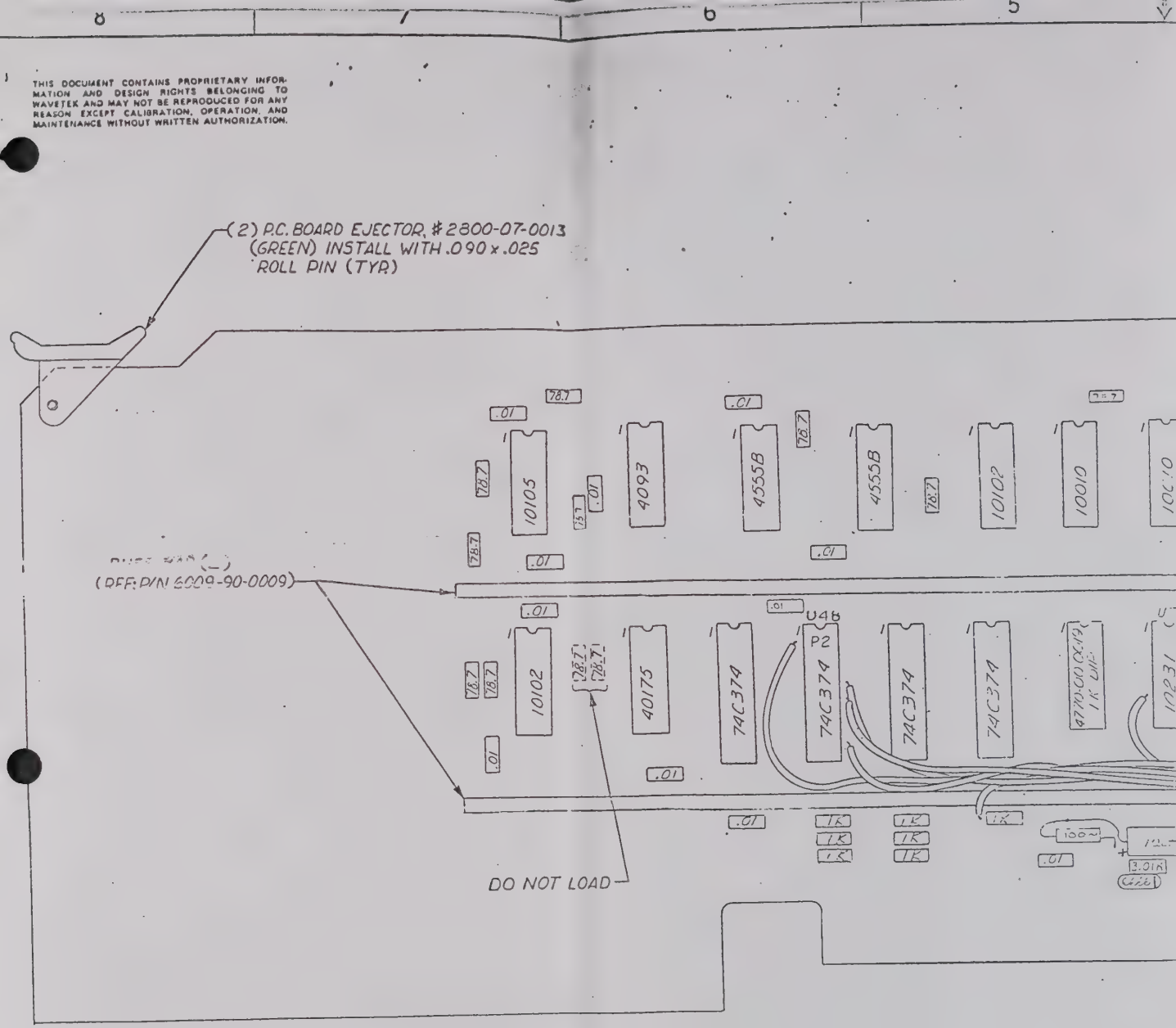
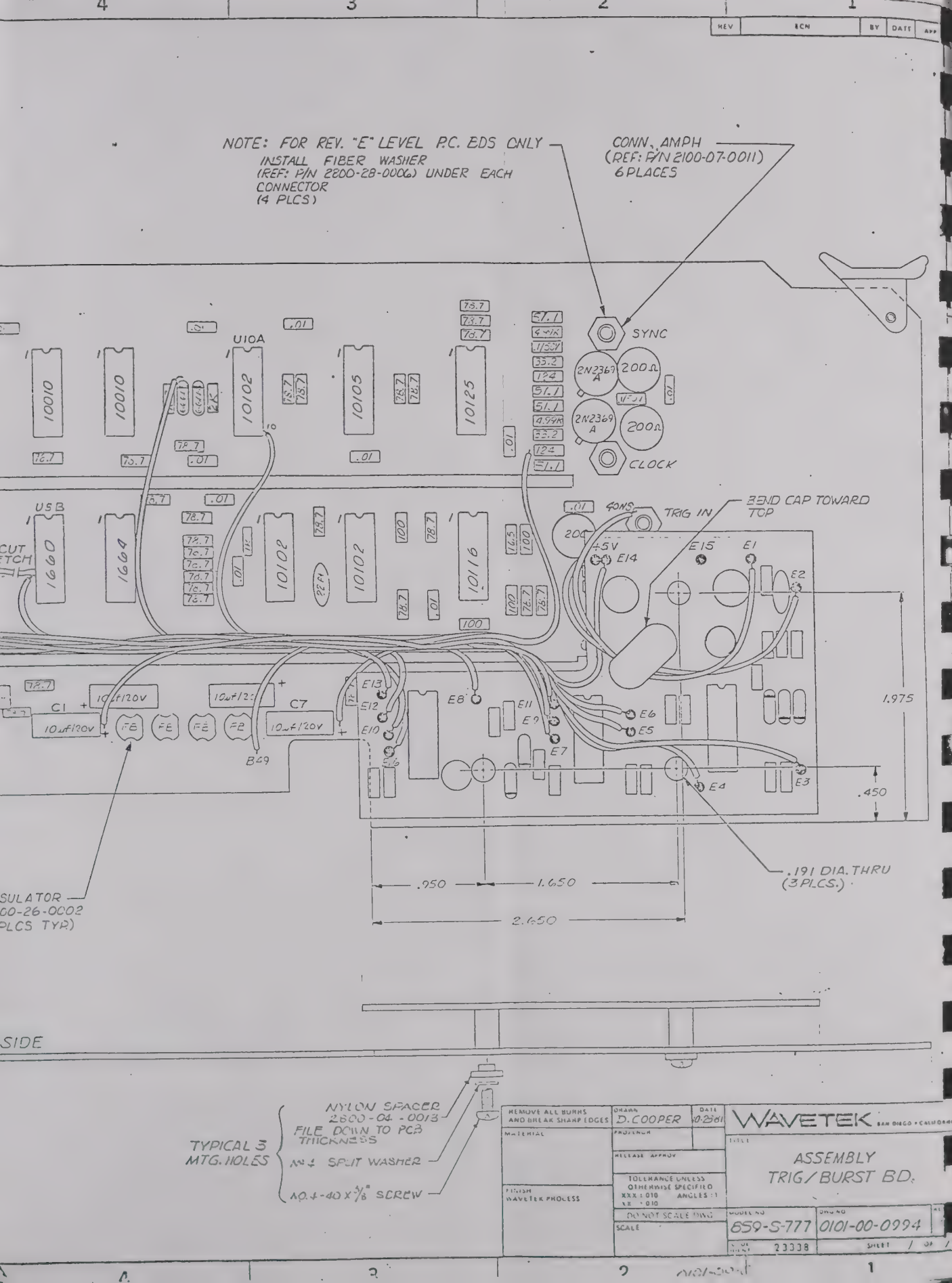


22 AWG ↓

ORIGIN	SIGNAL	COLOR	DESTINATION	
E1	COM	BLK	J4 (GND)	
E2	−15V	VIO	R42 (−15V)	
E3	−2V	RED	CR5 CATHODE	CR-5
E4	−5.2V	GRN	R24 (−5.2V)	
E5	A1	ORN	U4B PIN 15	P2-15
E6	A2	YEL	U4B PIN 16	P2-16
E7	A0	BLU	U4B PIN 12	P2-12
E8	MNTG	WHT	J6 PIN A11	
E9	A4	GRY	U4B PIN 2	P2-2
E10	TSYC1	WHT/BRN	U10A-10	U10A-10
E11	TDLY2	WHT/RED	J6 PIN B49	
E12	TSYC1&2	WHT/BLK	U6B PIN 6	UT8-6
E13	COM	BLK	C7 "+"	
E14	+5V	BRN	C1 "+"	
E16		ORN/WHT	U8B-8	

NOTE: UNLESS OTHERWISE SPECIFIED 1. USE TY-WRAP AS REQUIRED.



NOTE: FOR REV. "E" LEVEL P.C. BDS ONLY
INSTALL FIBER WASHER
(REF: P/N 2800-28-0006) UNDER EACH
CONNECTOR
(4 PLCS)
CONN. AMPH
(REF: P/N 2100-07-0011)
6 PLACES
SYNC
CLOCK
2N2369 A
200Ω
U10A
10010
10102
10105
10125
USB
1660
1664
10116
TRIG IN
BEND CAP TOWARD TOP
+5V
E14
E15
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
C1
C7
10µf/20V
B49
1.975
.450
.950
1.650
2.650
.191 DIA. THRU
(3 PLCS.)
SULATOR
00-26-0002
PLCS TYP)
SIDE
NYLON SPACER
2800-04-0013
FILE DOWN TO PCB
THICKNESS
TYPICAL 3
MTG. HOLES
No 4 SPLIT WASHER
NO. 4-40 X 3/8" SCREW
REMOVE ALL BURRS
AND BREAK SHARP EDGES
MATERIAL
FINISH
WAVETEK PROCESS
DRAWN
D. COOPER
DATE
10-23-81
PROJ ENGR
RELEASE APPROV
TOLERANCE UNLESS
OTHERWISE SPECIFIED
XXX ± .010 ANGLES ± 1
XX ± .010
DO NOT SCALE DWG
SCALE
WAVETEK
SAN DIEGO • CALIFORNIA
TITLE
ASSEMBLY
TRIG/BURST BD.
MODEL NO
859-S-777
DWG NO
0101-00-0994
23338
SHEET 1 OF 1

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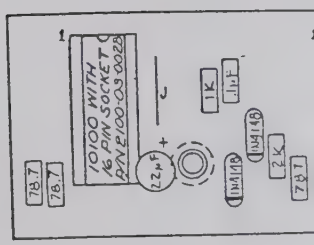
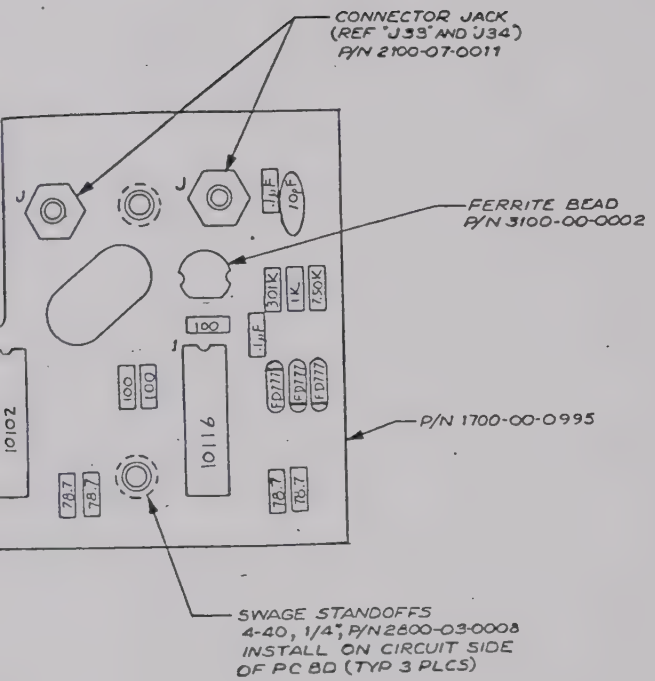


NOTE: UNLESS OTHERWISE SPECIFIED



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN I. Chow	DATE 10/23/90	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR		TITLE ASSEMBLY 2ND CHANNEL TRIGGER BOARD
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG		MODEL NO 859-S-777 DWG NO 0101-00-0995 REV A
	SCALE		LOCK IDENT 23338 SHEET 1 OF 1

4 3 2 1

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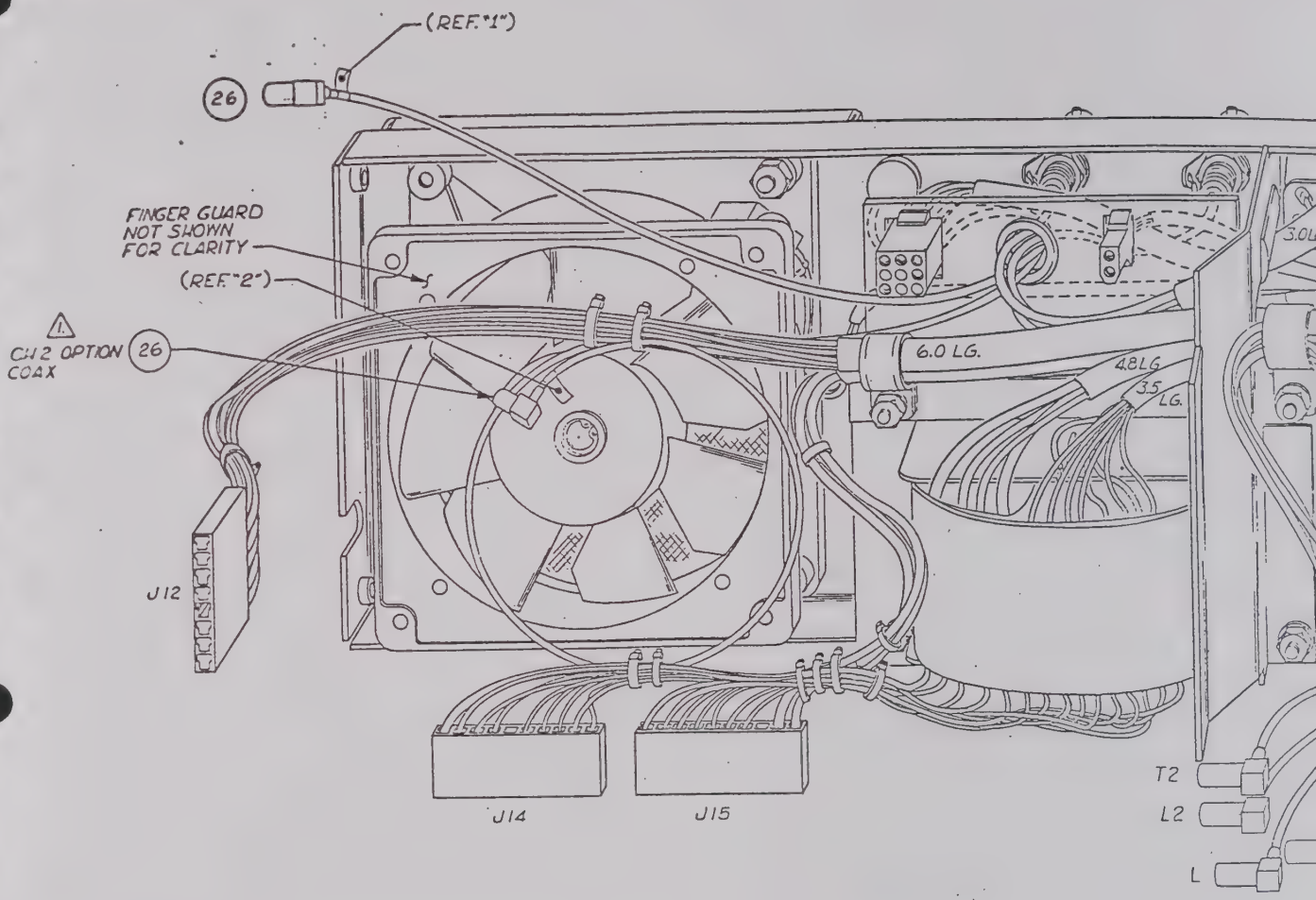
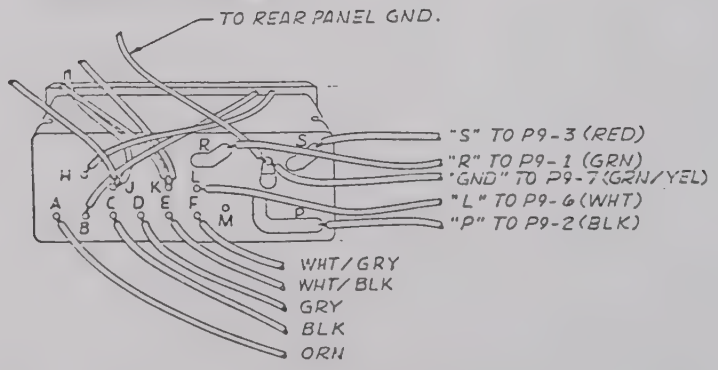


CORCOM WIRING



3. COLOR OF PIGTAIL OF COAXES SHOULD REFLECT THEIR LENGTH (PER WAVETEK STANDARDS ASSEMBLY MANUAL.)

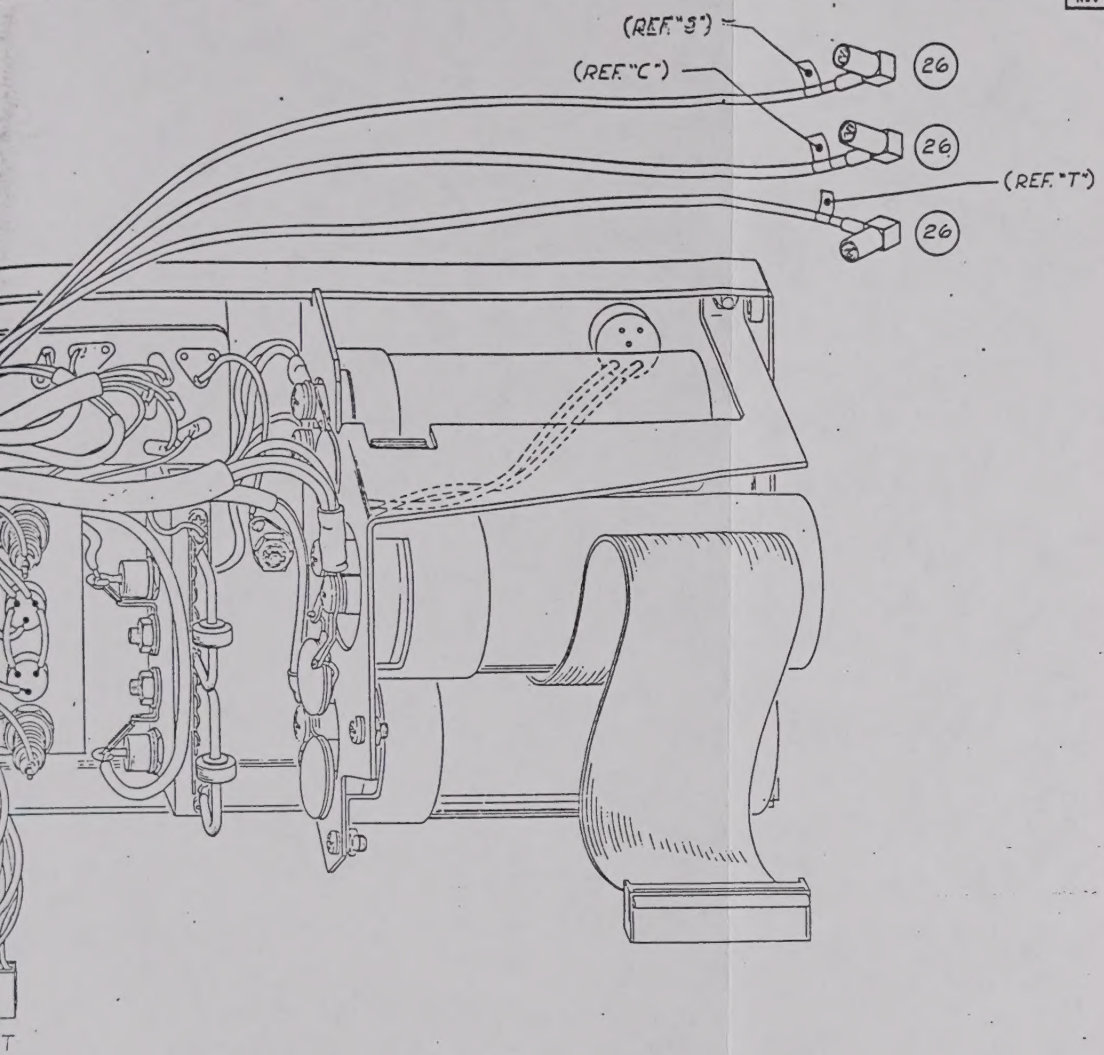
2. ALL WIRE LENGTHS ARE APPROX.

1 INSTALL TY-WRAPS AS SHOWN.

NOTE: UNLESS OTHERWISE SPECIFIED

A

REV	ECN	BY	DATE	APP



REAR PANEL BNC CONNECTORS

	P/L ITEM NO	FROM	TO	WIRE	LG.	FUNCTION	MK
	26	J23	A9-J1	RG174 U	20"	CH1 OUTPUT	1
	26	J24	A16-J1	RG174/U	20"	CH2 OUTPUT	2
	26	J25	A4-J2	RG174/U	12"	CLOCK OUT	C
⚠1	26	J26	A4-J3	RG174/U	12"	SYNC OUT	S
REMOVED	~~26~~	~~J27~~	~~A4-J4~~	~~RG174/U~~	~~14"~~	~~TRIG IN~~	~~T~~
	26	E30	A4-J1	RG174/U	8"	TRIG LEVEL	L

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 9-28-7	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE ASSEMBLY REAR PANEL 859-S-777
	RELEASE APPROV R. CONERO 4/8/80		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO.	DWG NO. 0102-00-0672-1 REV W
	SCALE	CODE IDENT 23338	1